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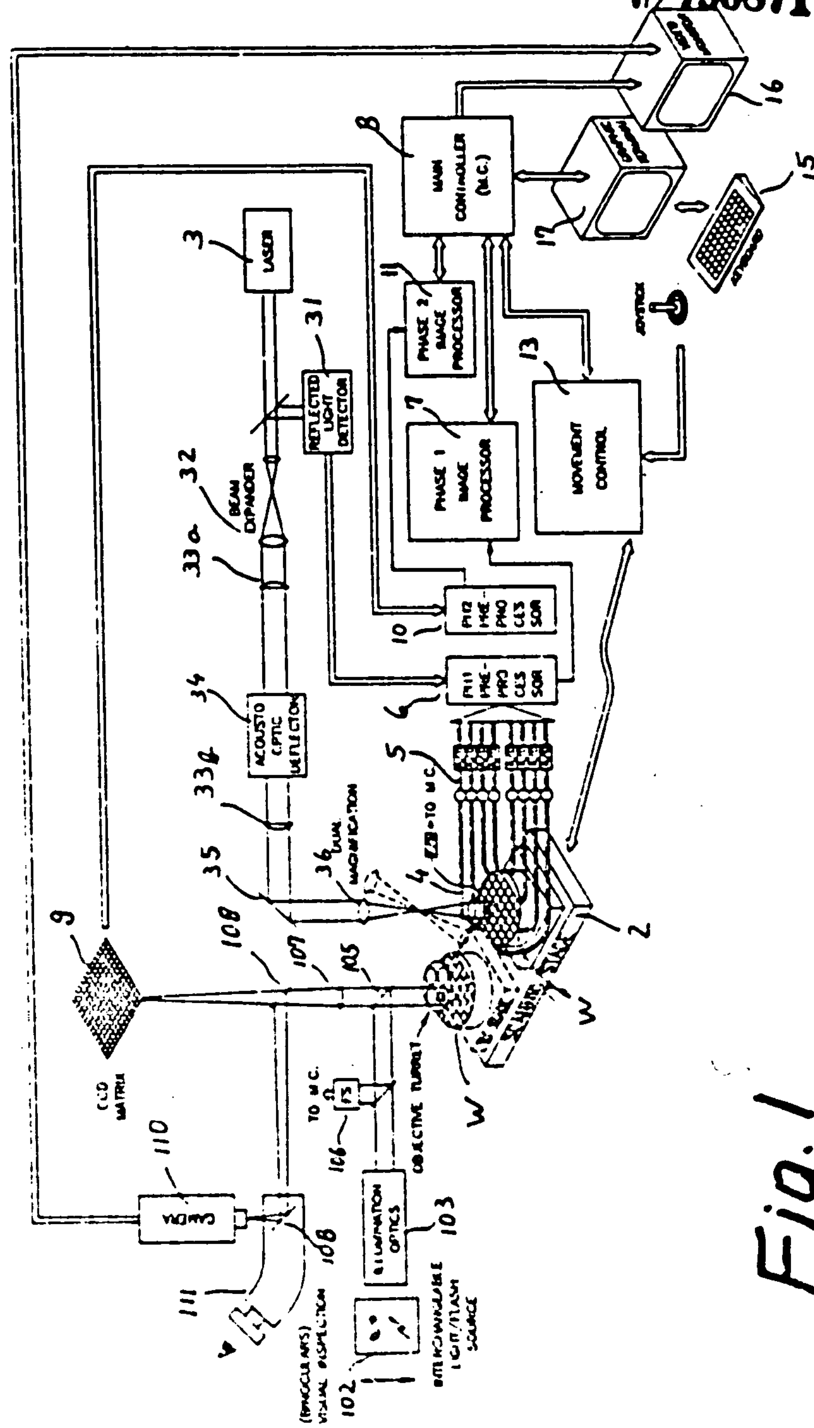

Fig. 1

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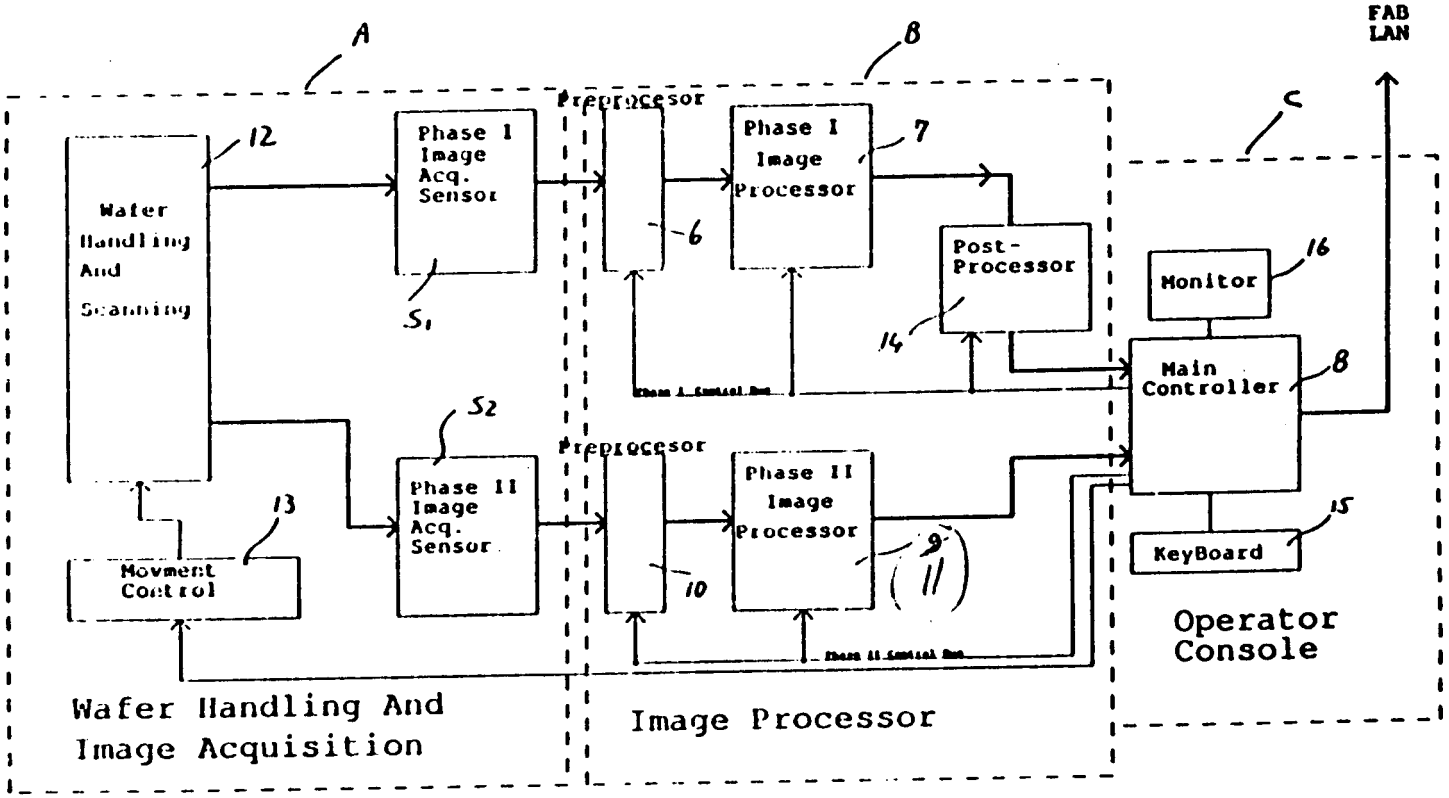


System Block Diagram

Fig. 2

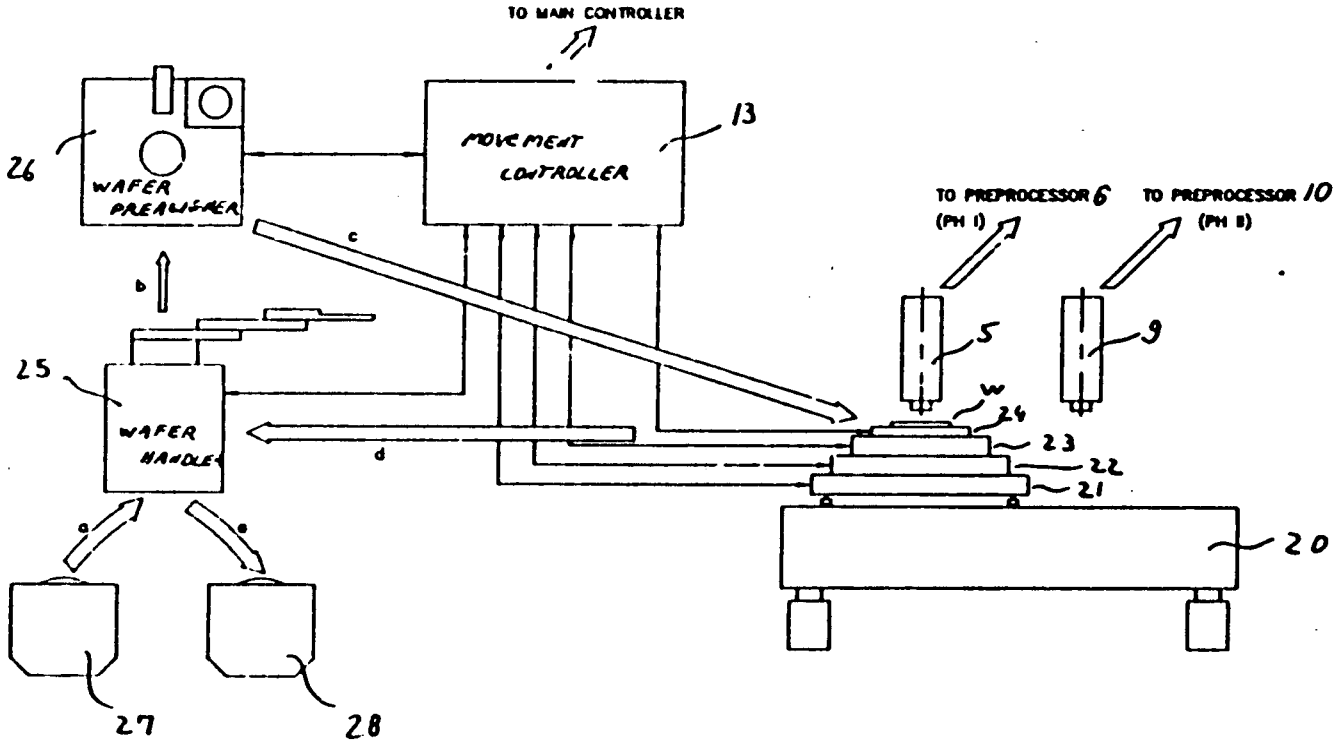
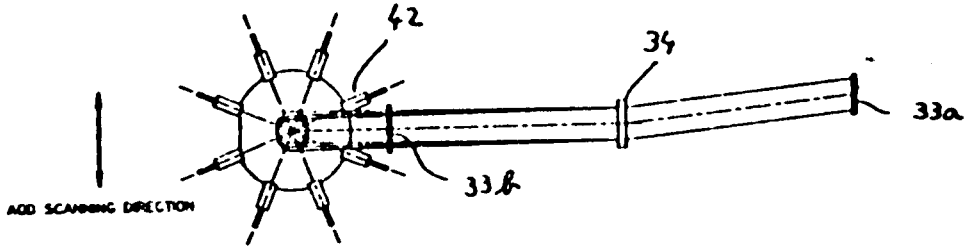


Fig 3

Fig 5



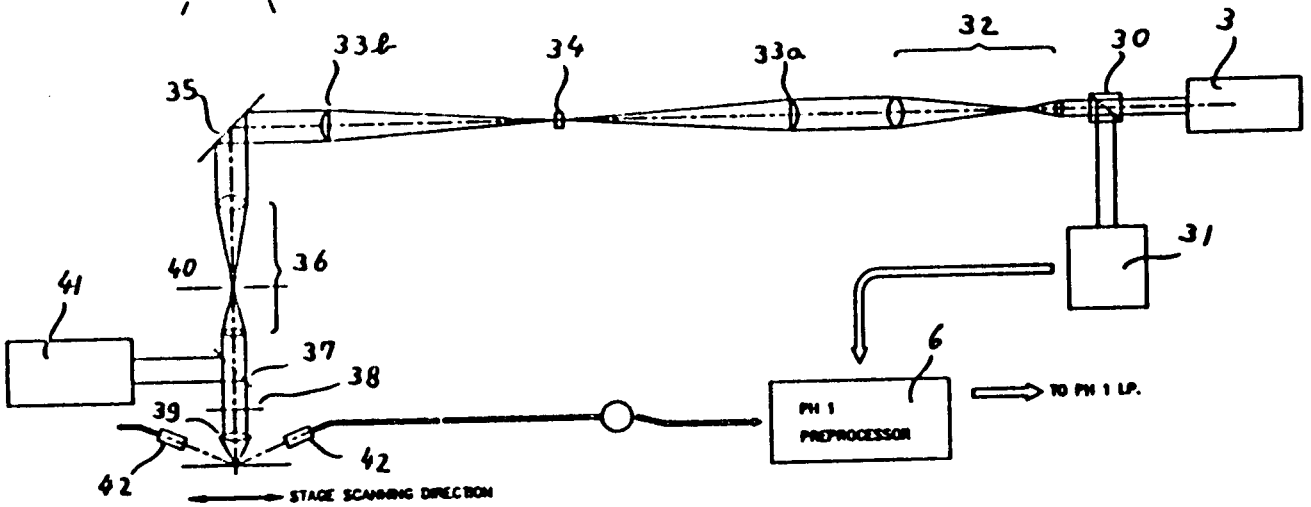


Fig. 4

Fig 6

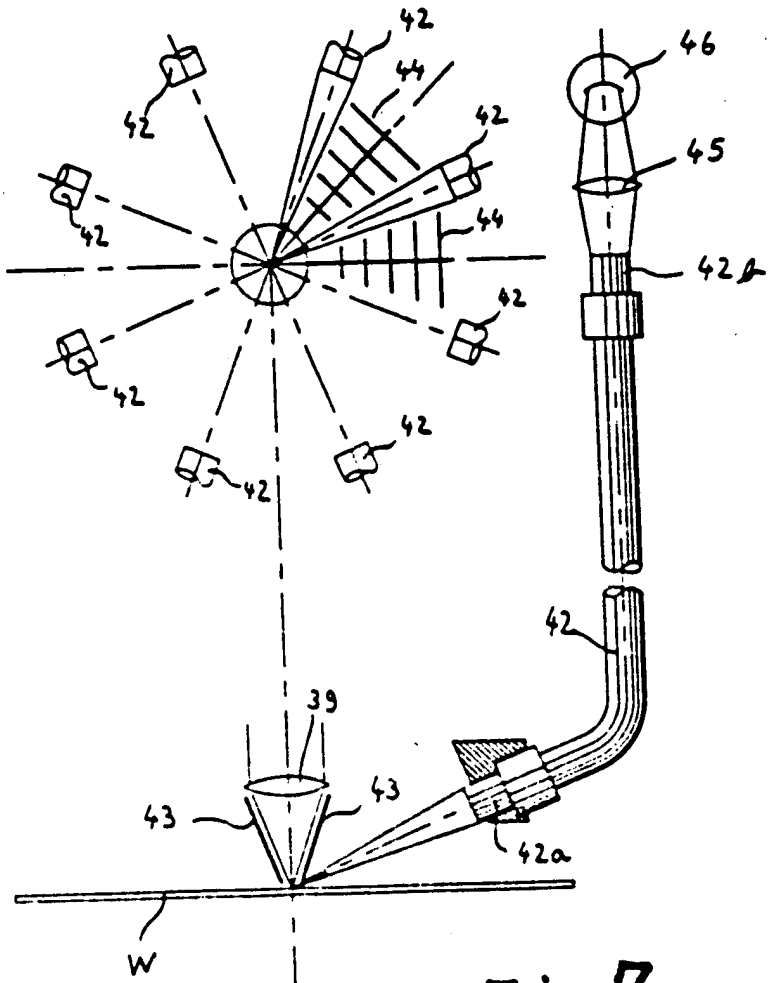


Fig. 7

11/790871

Fig 6a

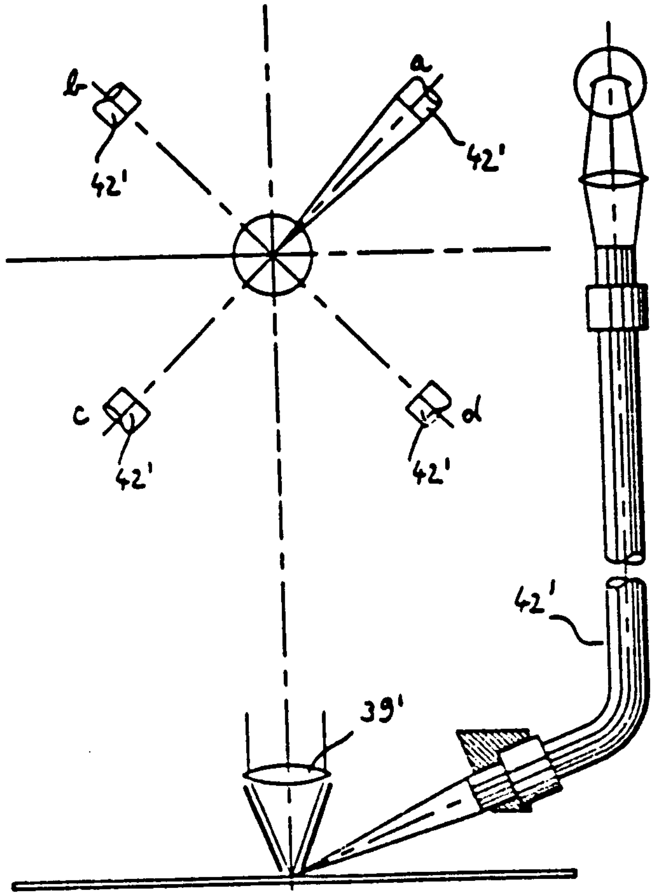
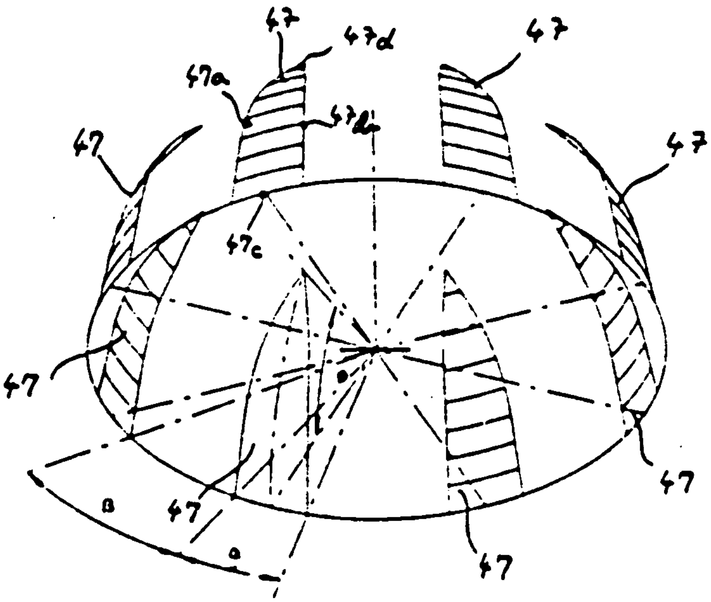


Fig 7a

11/790871

Fig. 8



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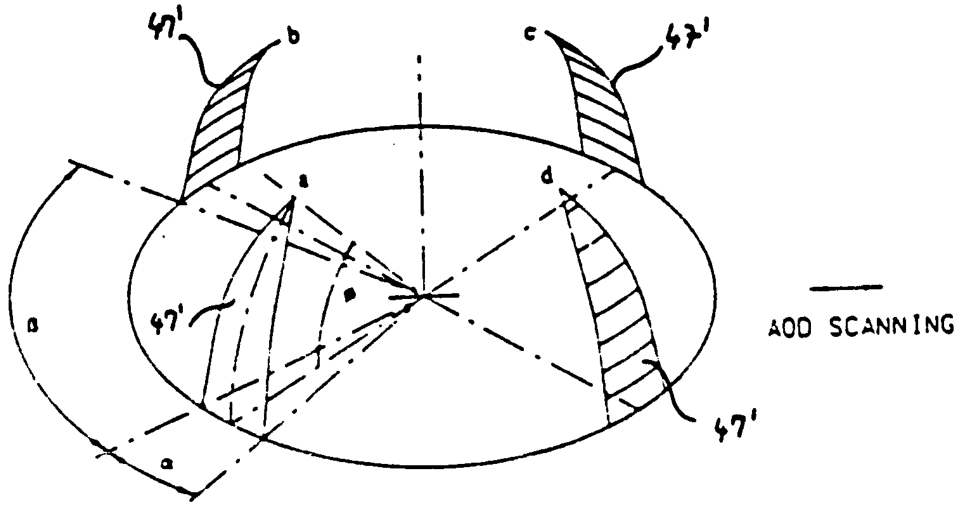


Fig 8a

11/790871

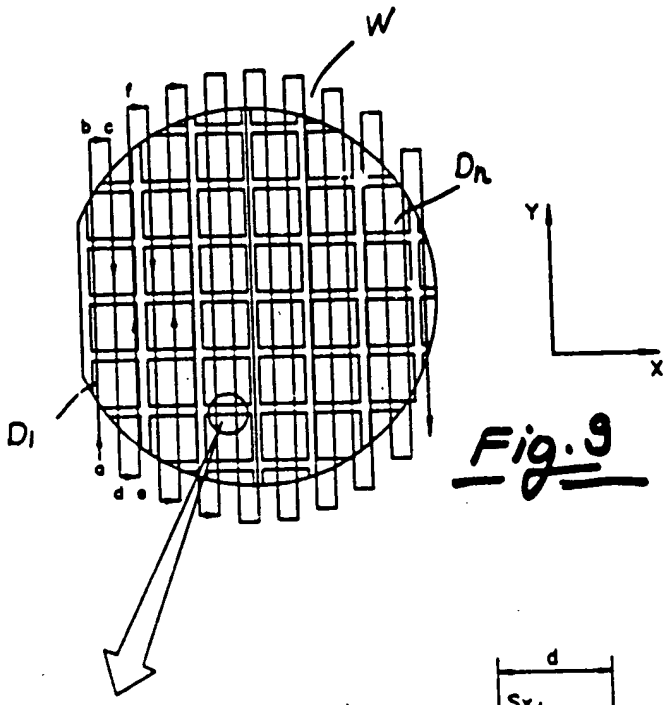


Fig. 9

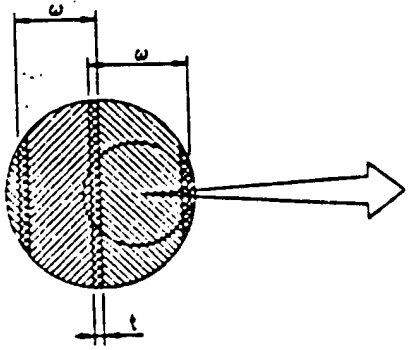


Fig 10

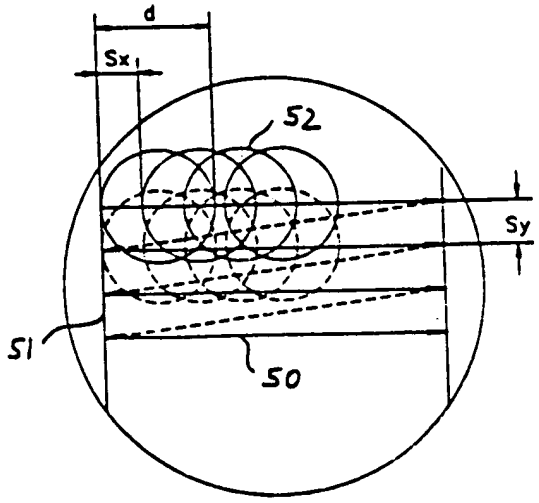


Fig. 11

Phase 1 I.P. OverAll Functional Block Diagram

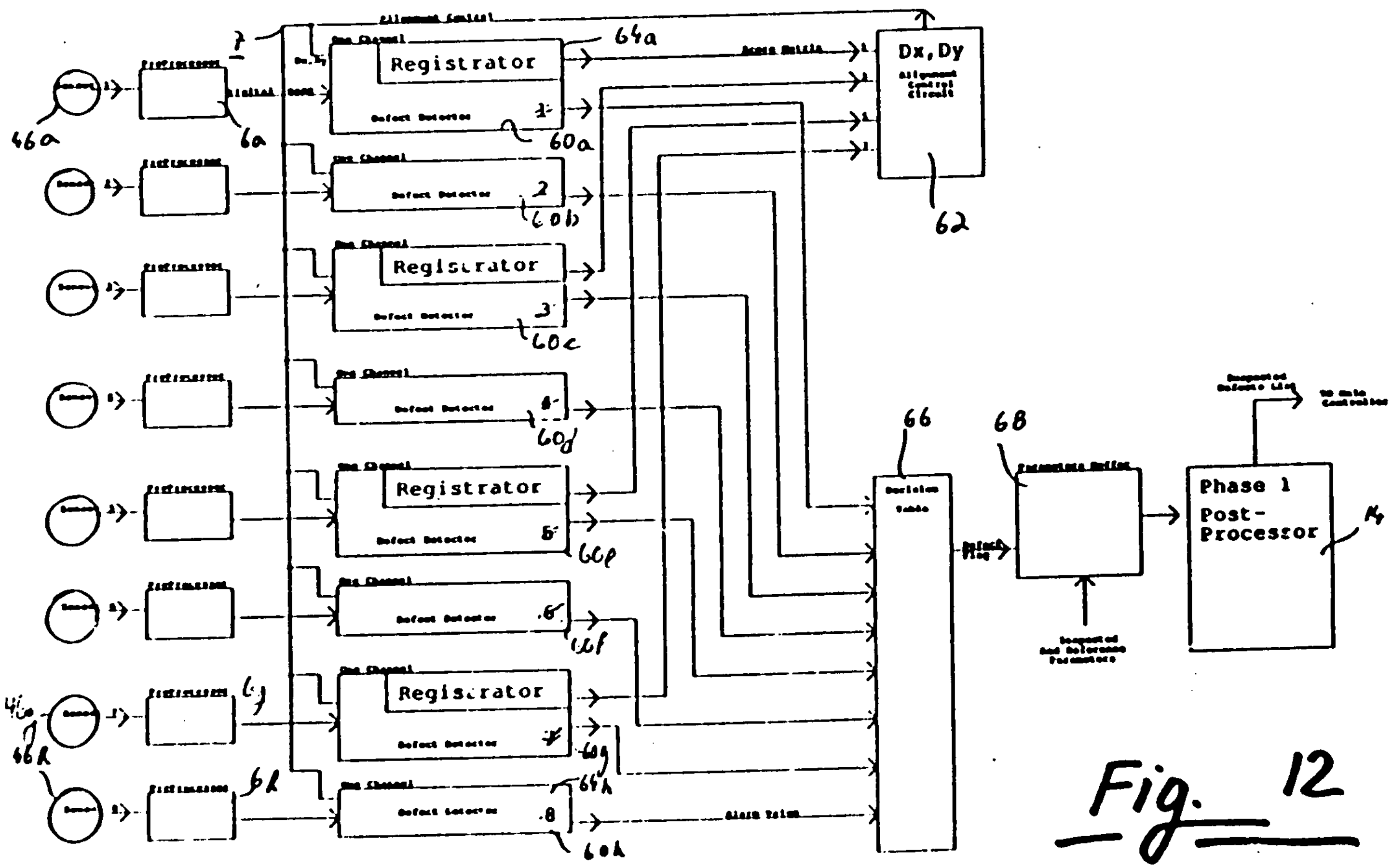


Fig. 12

11/790871

10/91

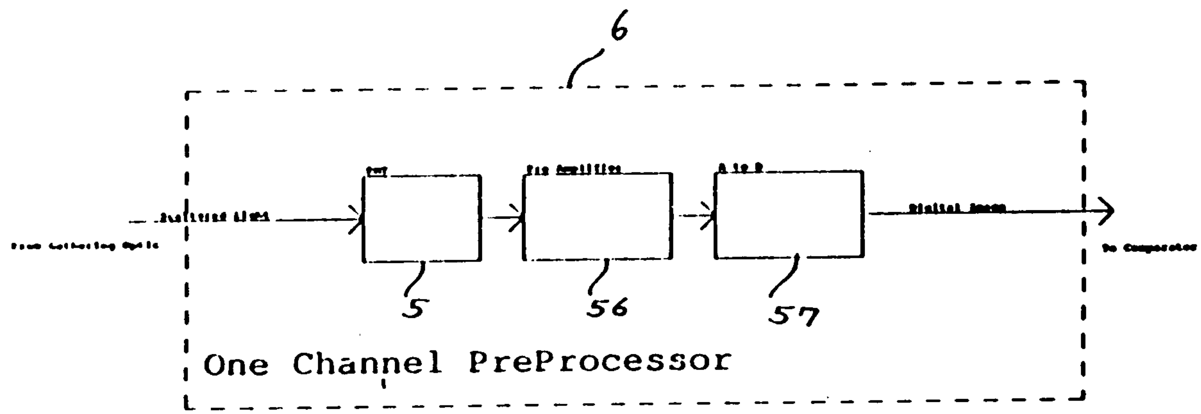
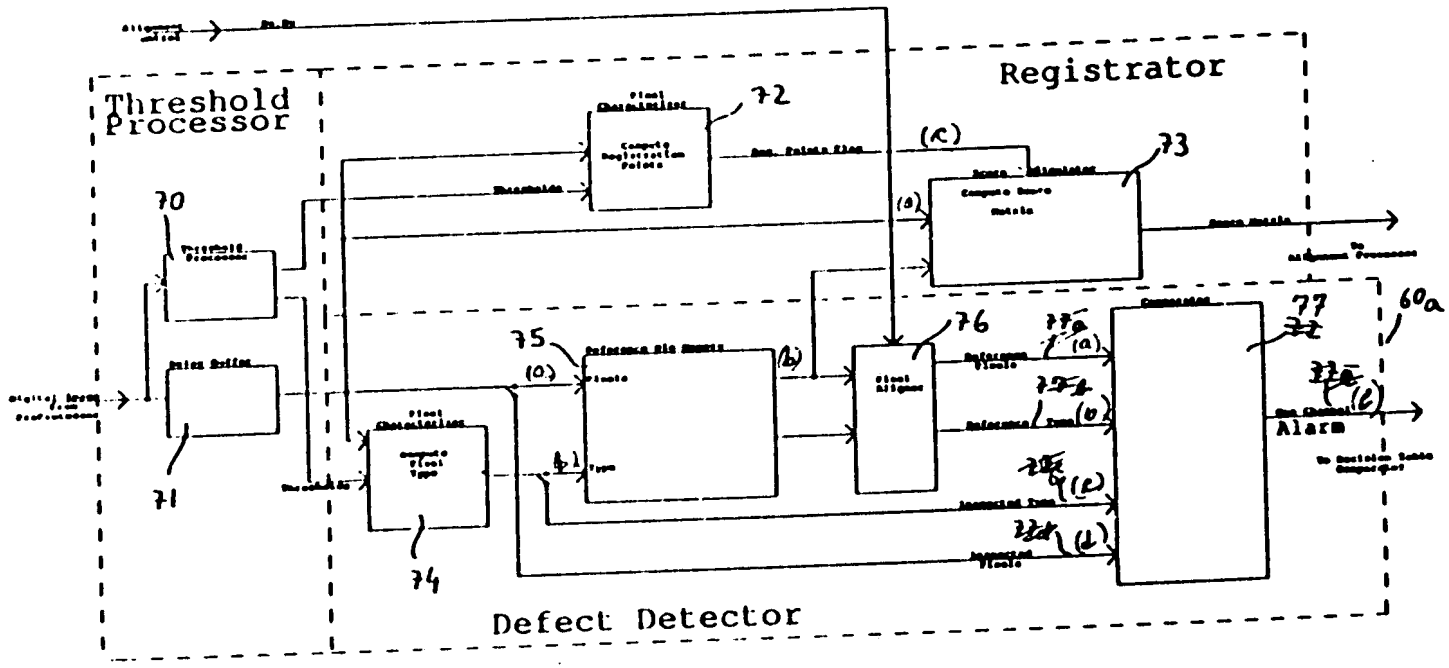


Fig. 13



One Channel I.P. Block Diagram

Fig. 14

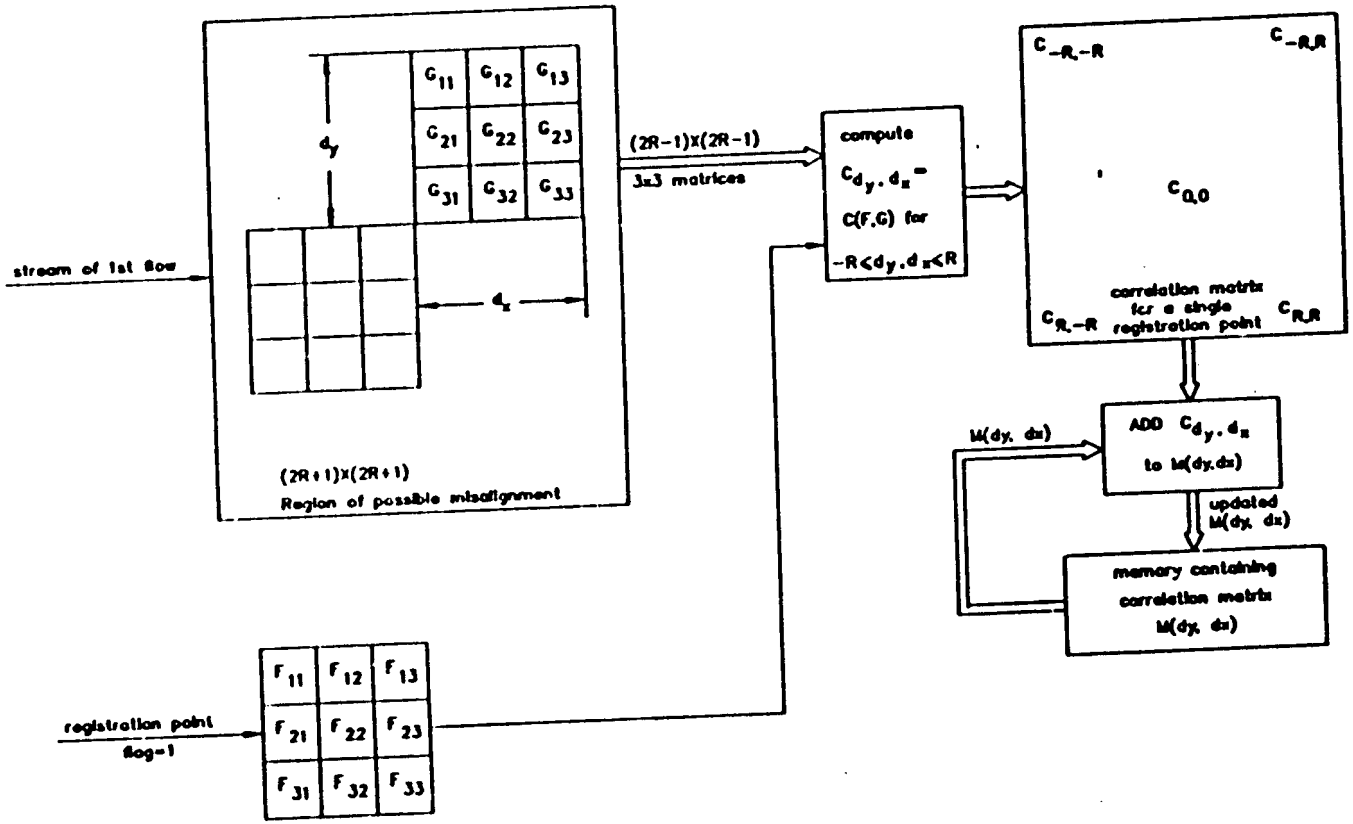
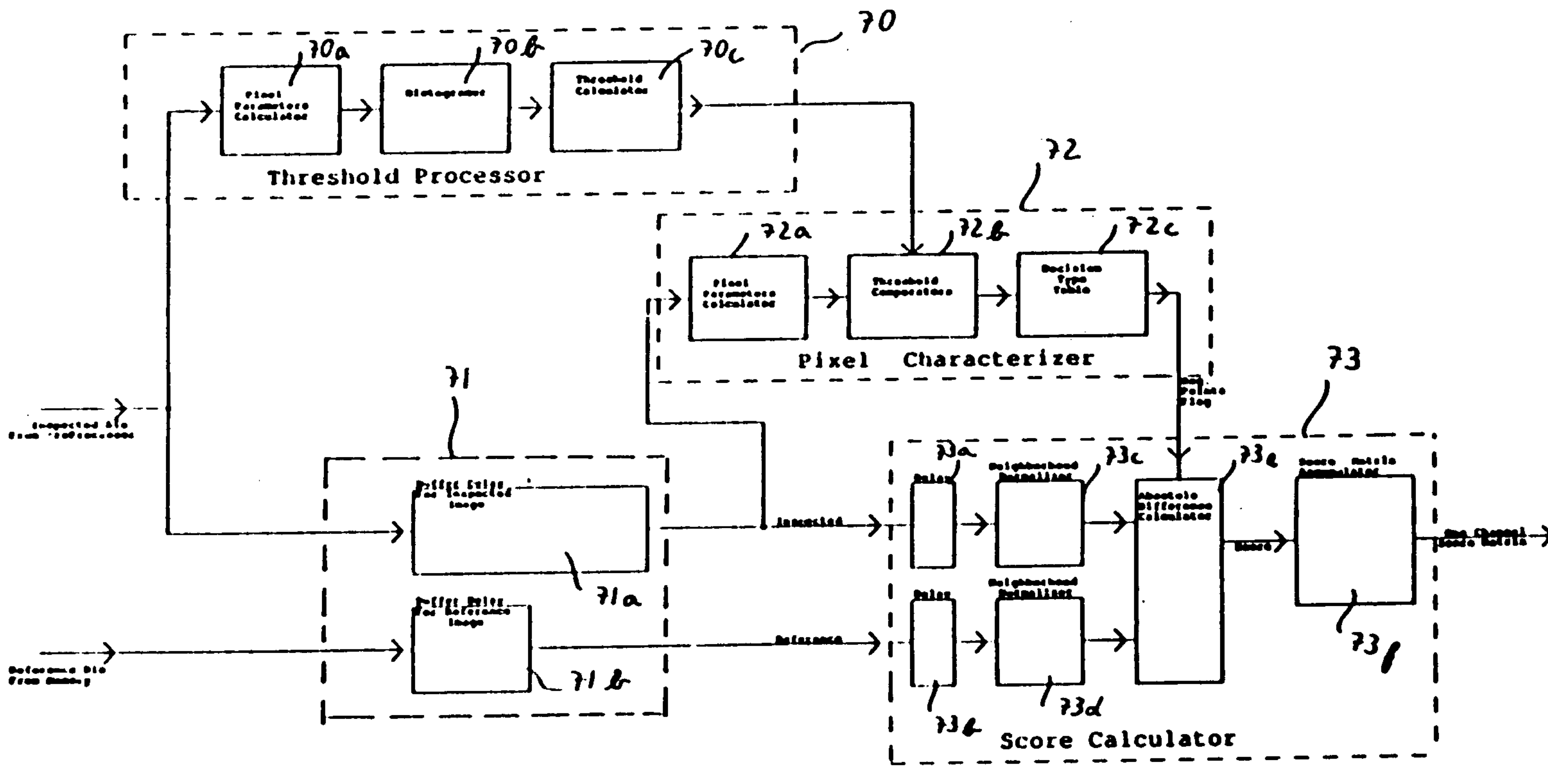


Fig. 14a

11/790871



Registrator Block Diagram

Fig. 15

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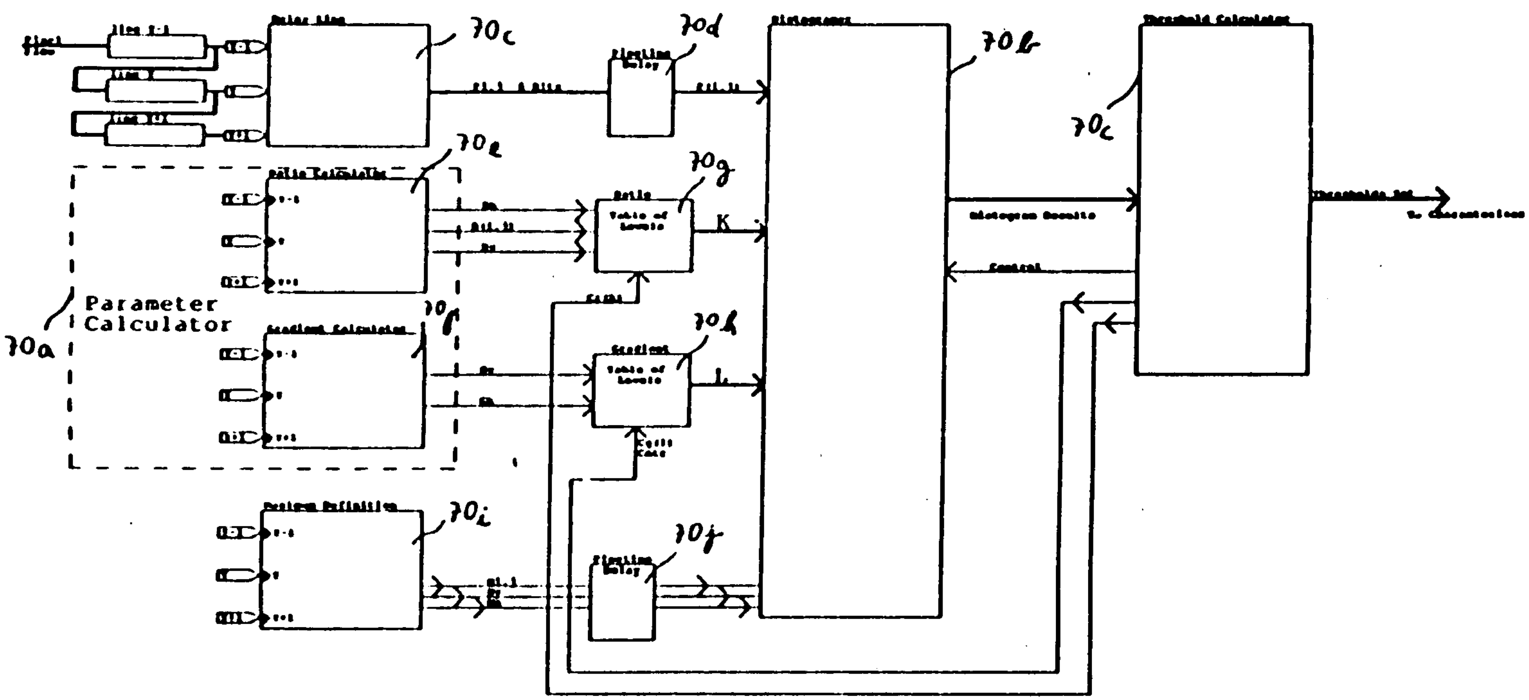

Threshold Processor Block Diagram

Fig. 16

11/790871

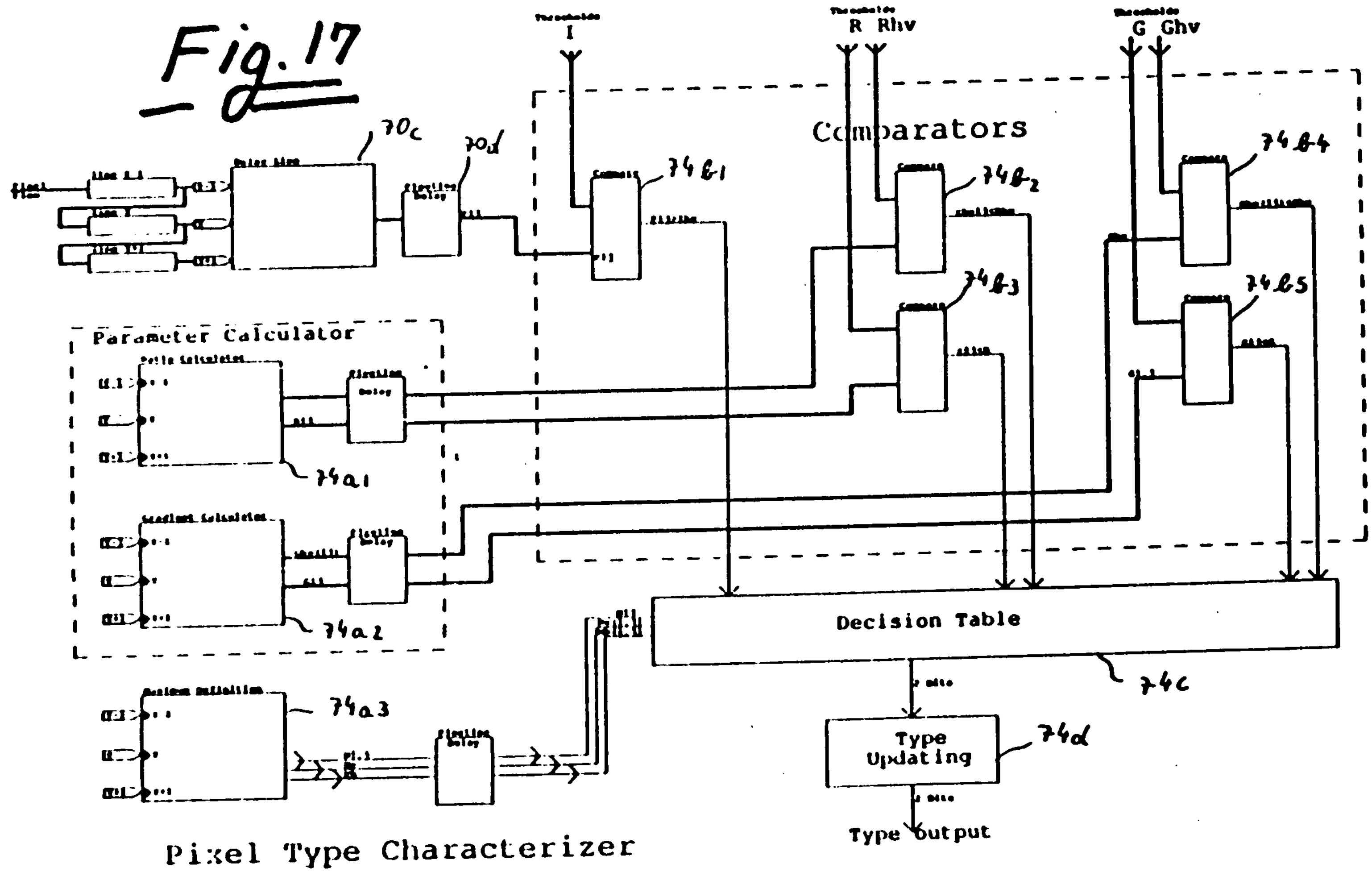

Fig. 17

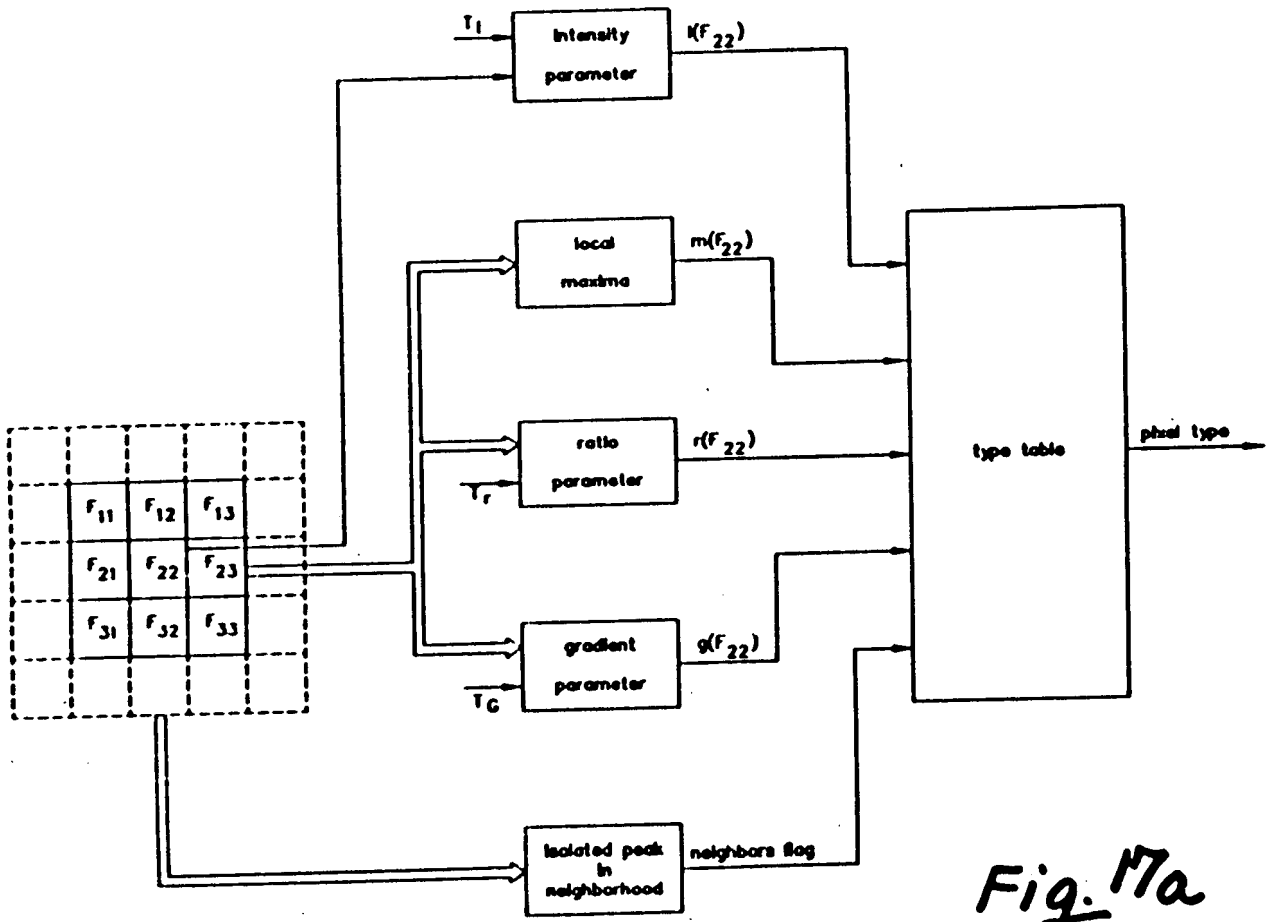

Fig. 17a

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Fig. 21a

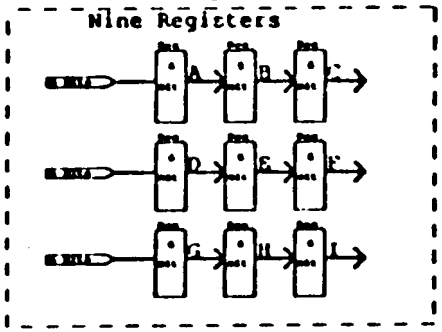
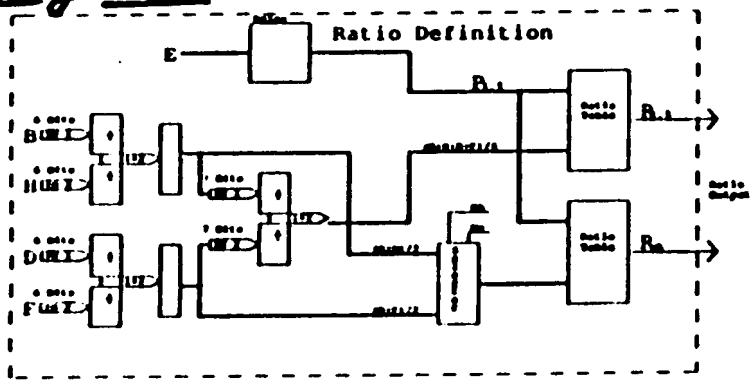


Fig. 18



Ratio And Maximum Definition

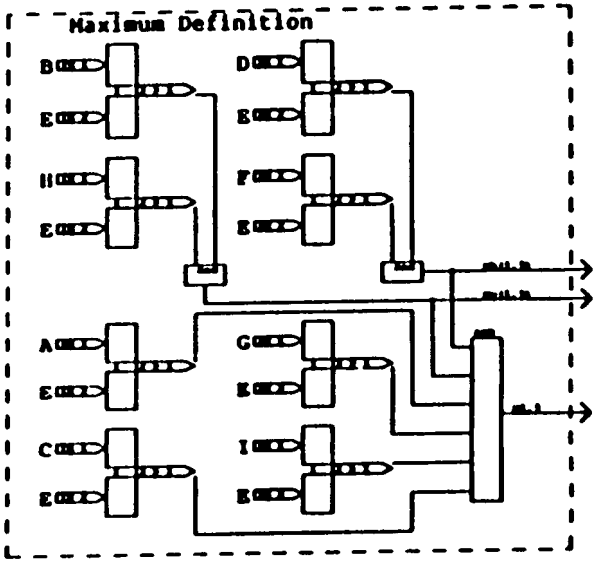


Fig. 20

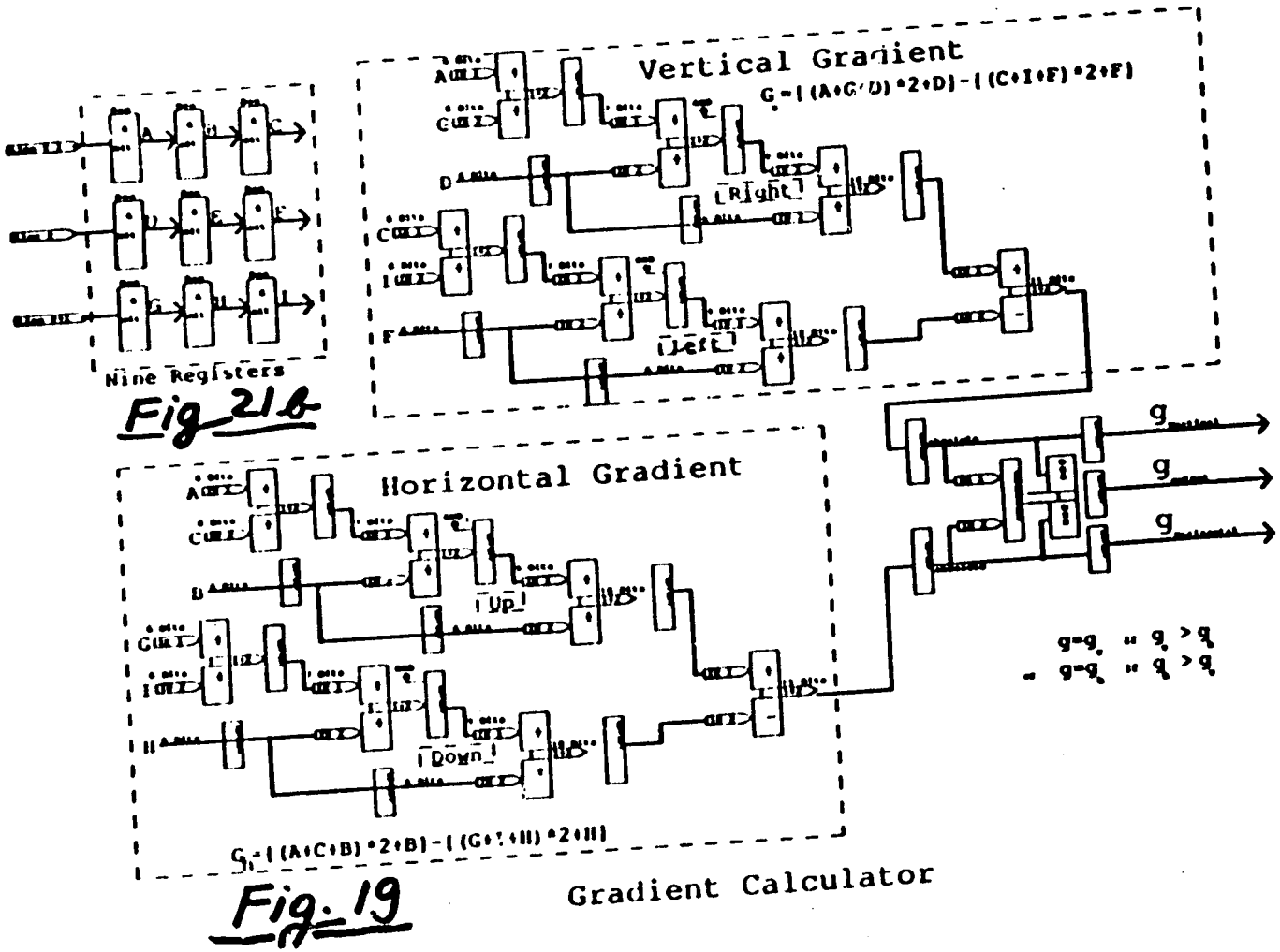
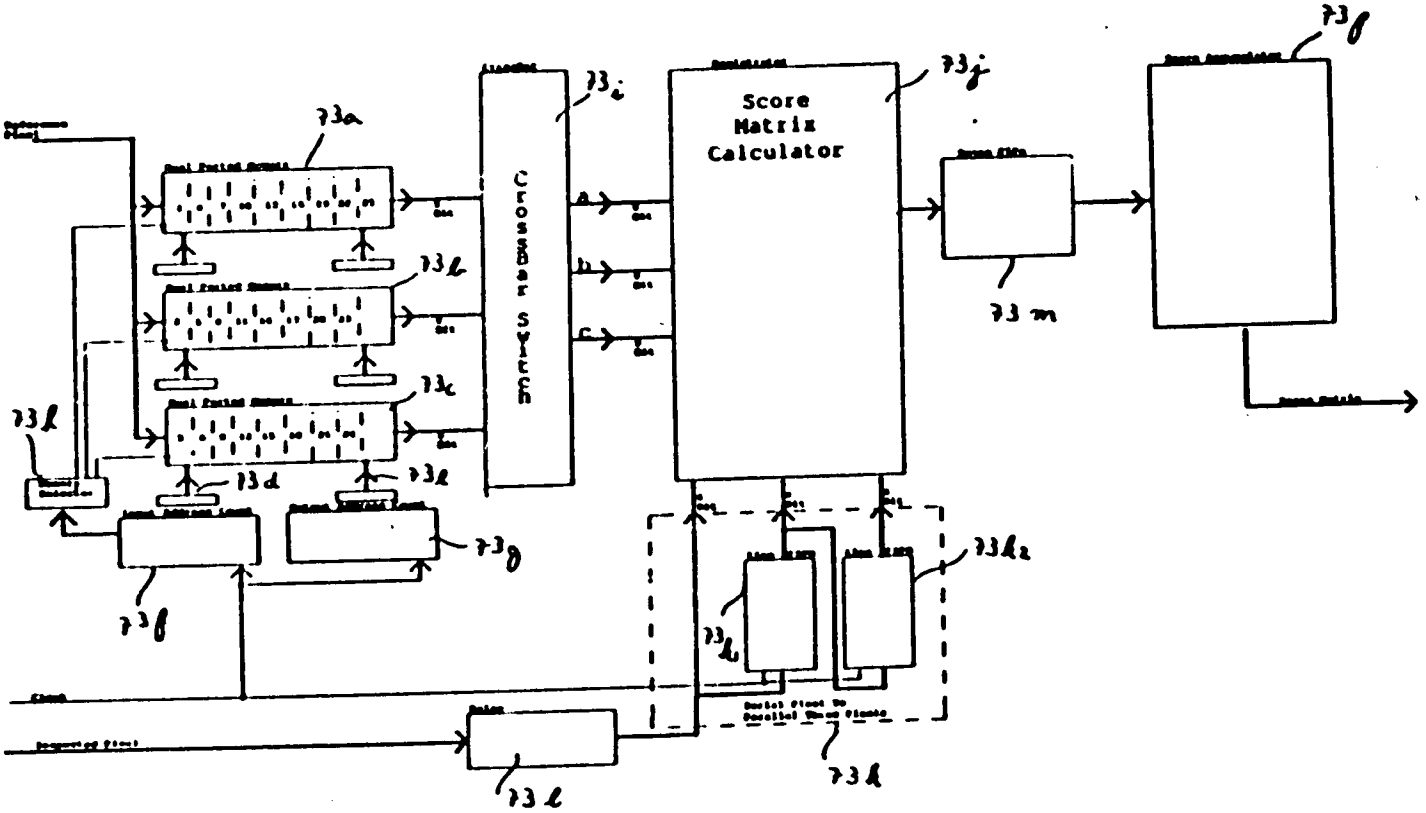


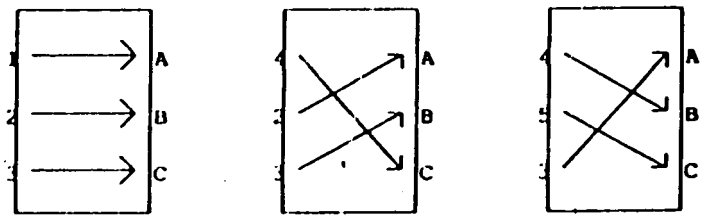
Fig 21b

Fig. 19



Registration Score Matrix Calculator

Fig. 22



CrossBar Switch Combination

Fig. 22a

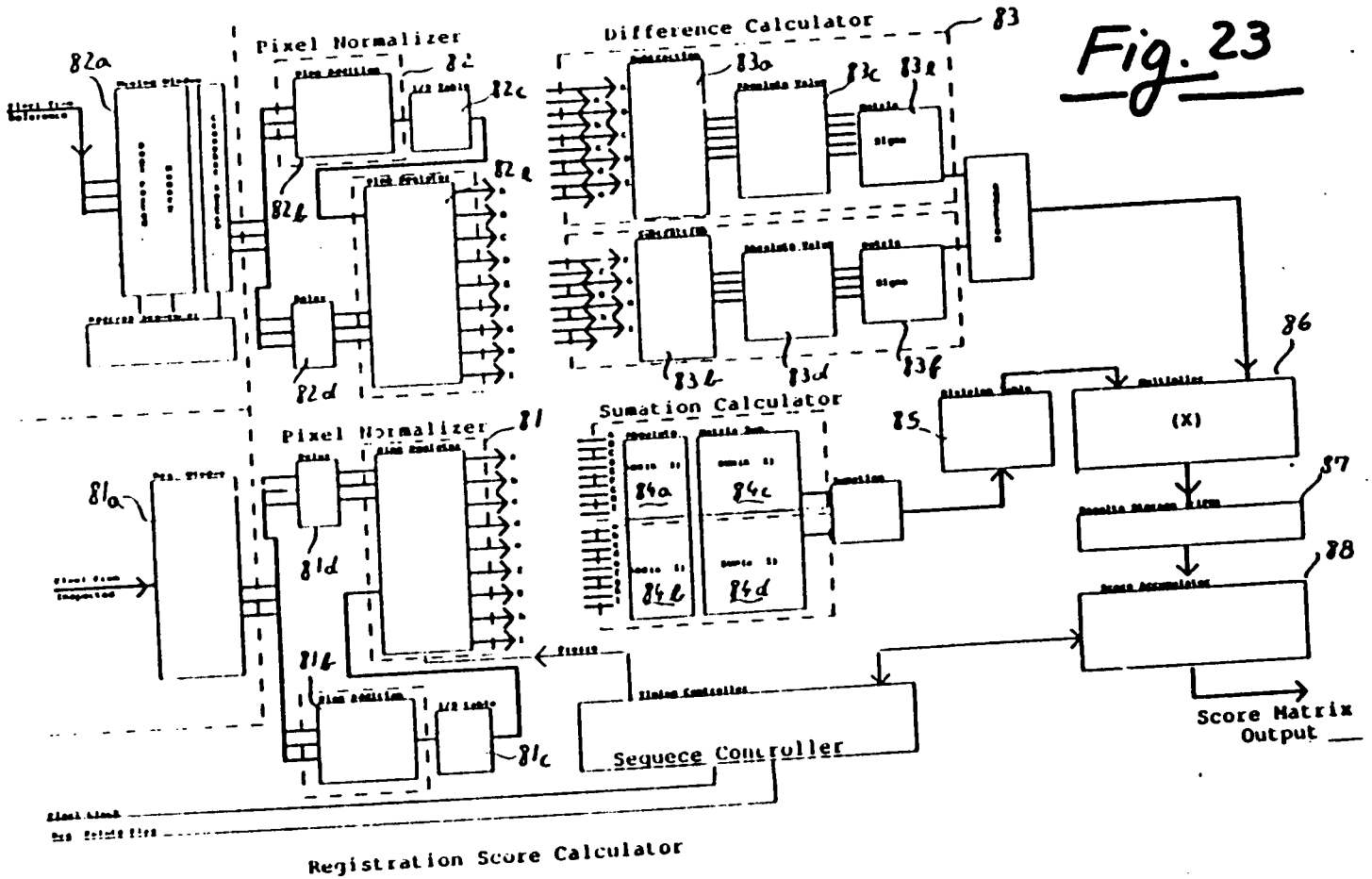


Fig. 23

11/79871

23/41

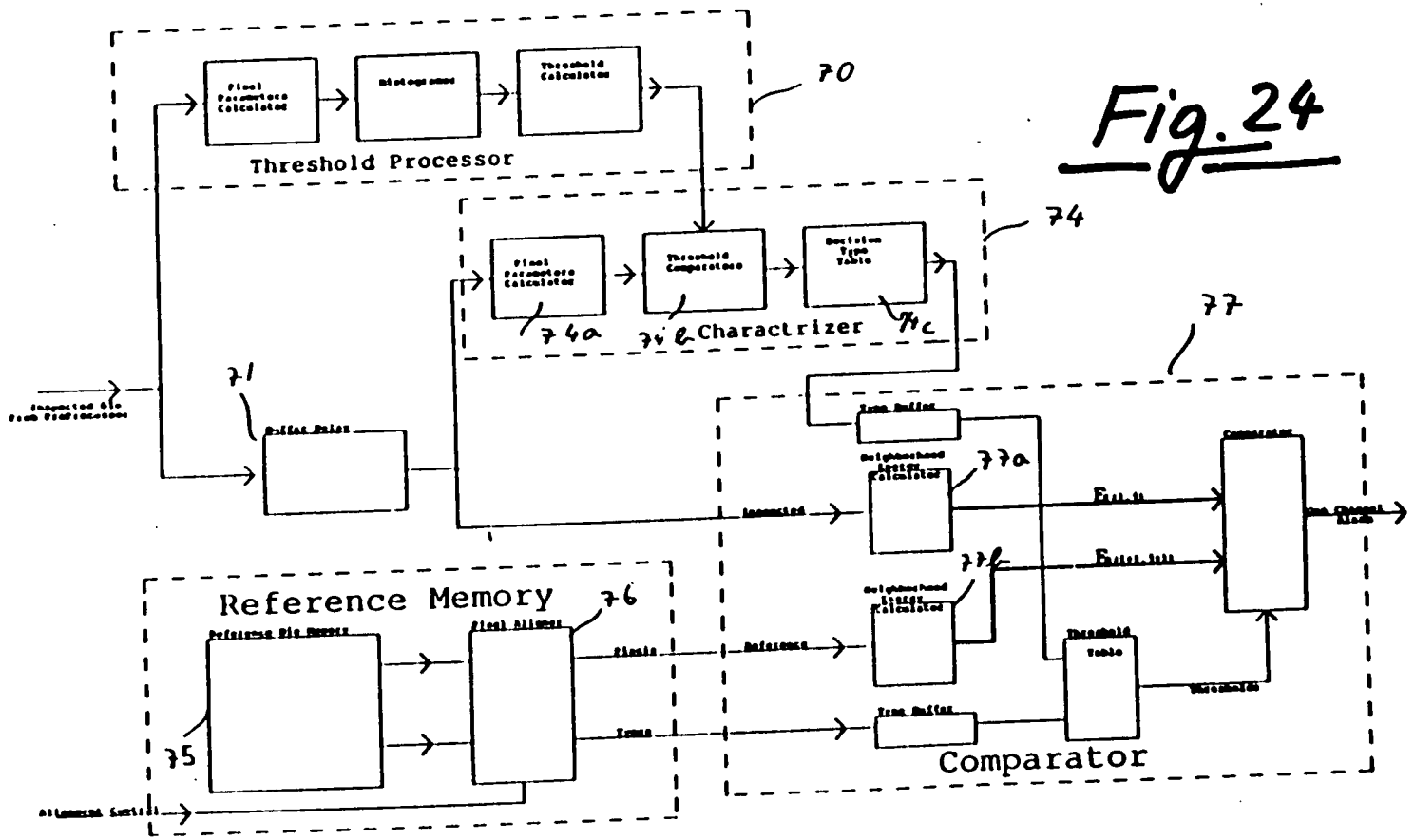


Fig. 24

Defect Detector Block Diagram

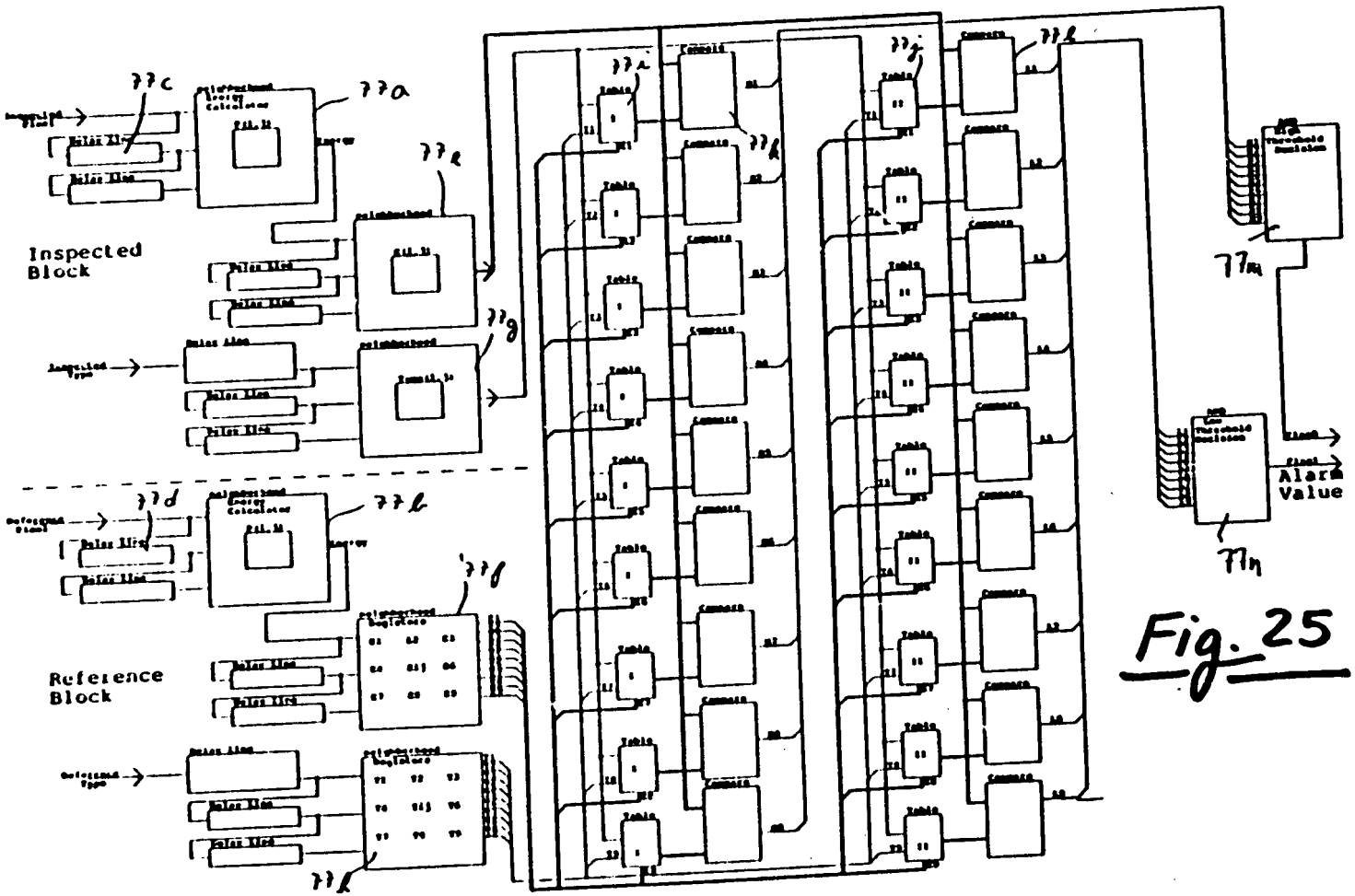


Fig. 25

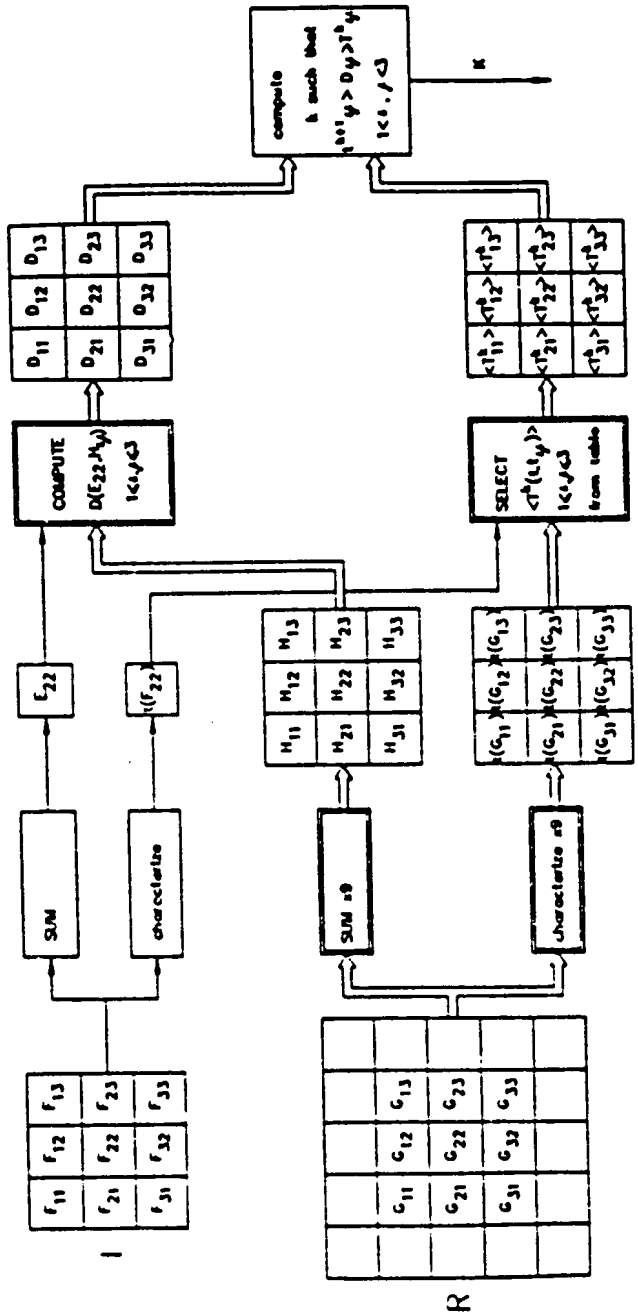

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Fig. 25a

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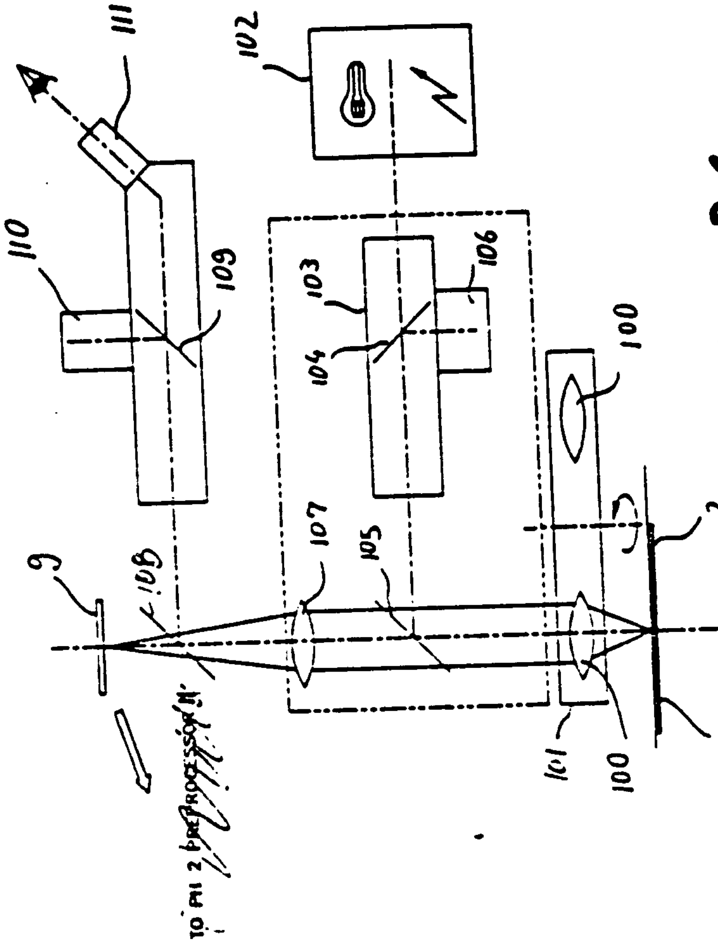

Fig. 26

11/790871

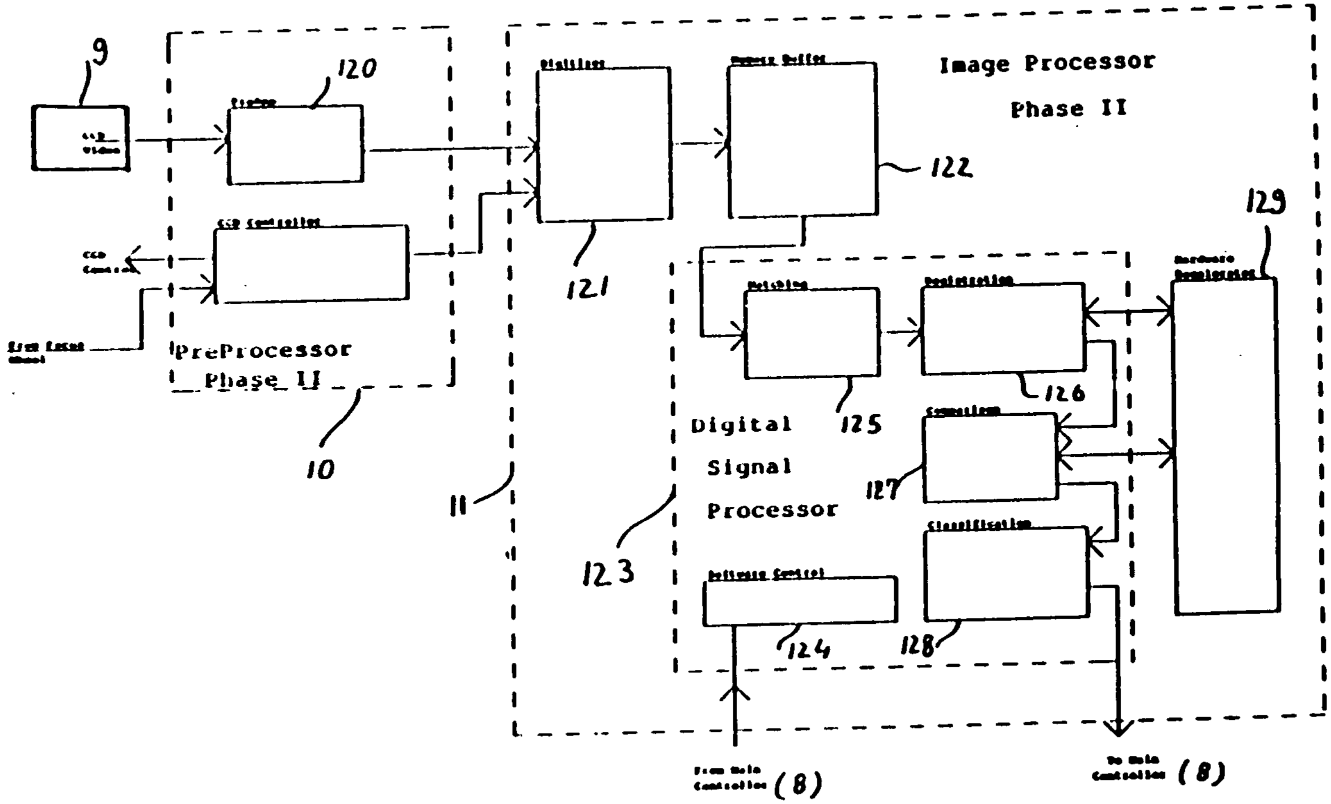

Fig. 27

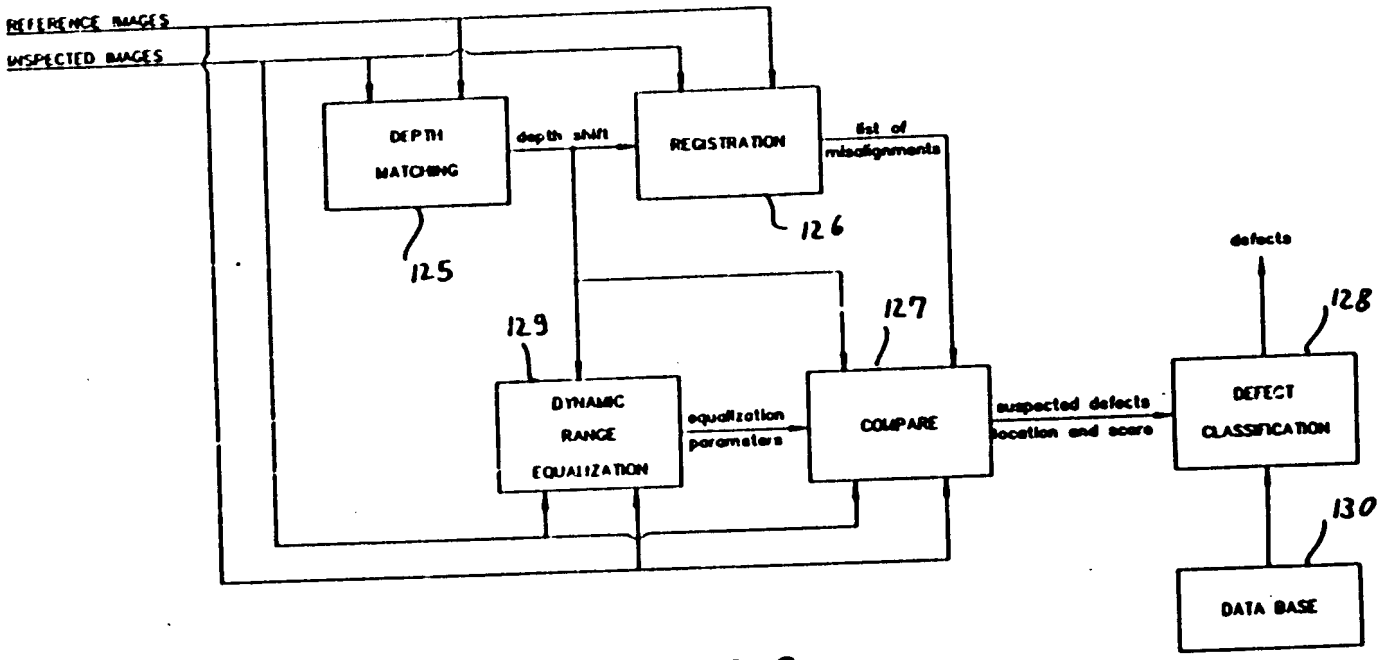
REFERENCE IMAGES
INSPECTED IMAGES
DEPTH MATCHING
depth shift
REGISTRATION
list of misalignments
125
126
129
127
DYNAMIC RANGE EQUALIZATION
equalization parameters
COMPARE
suspected defects location and score
defects
128
DEFECT CLASSIFICATION
130
DATA BASE

Fig. 28

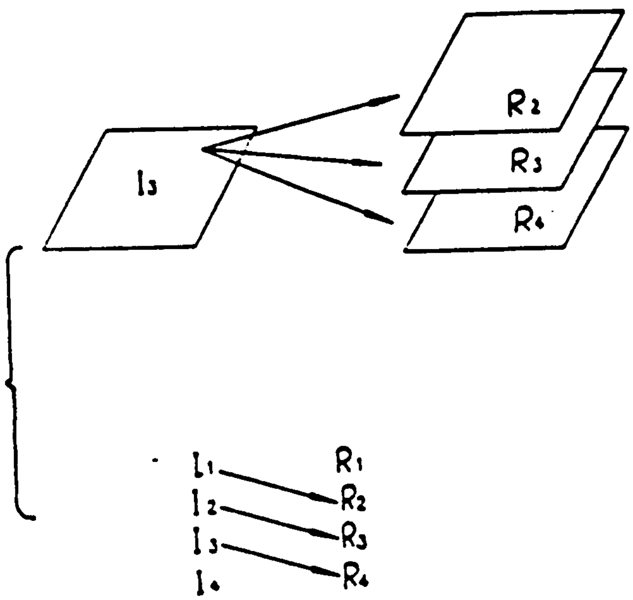

Fig. 29

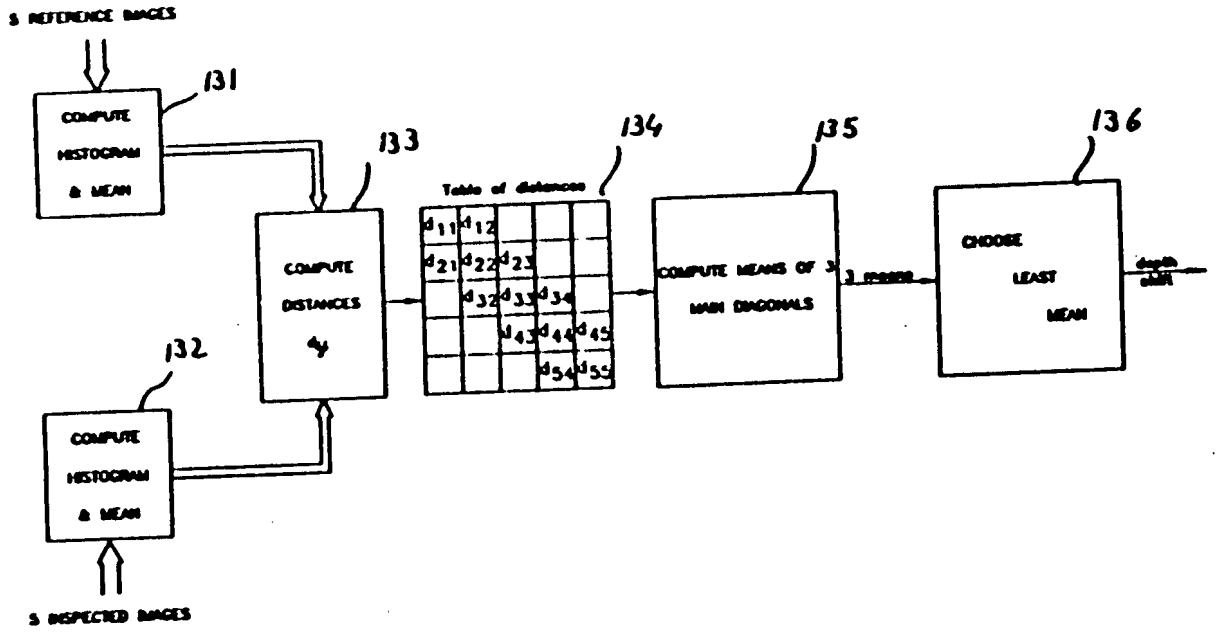

Fig. 30

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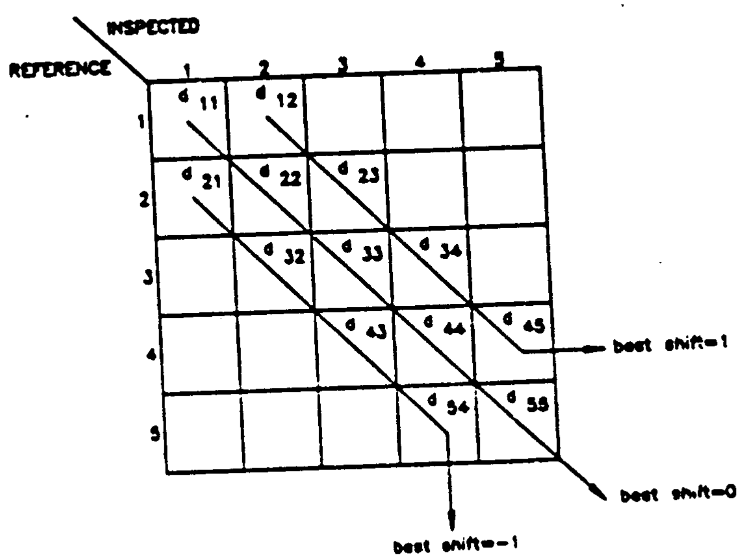

Fig. 31

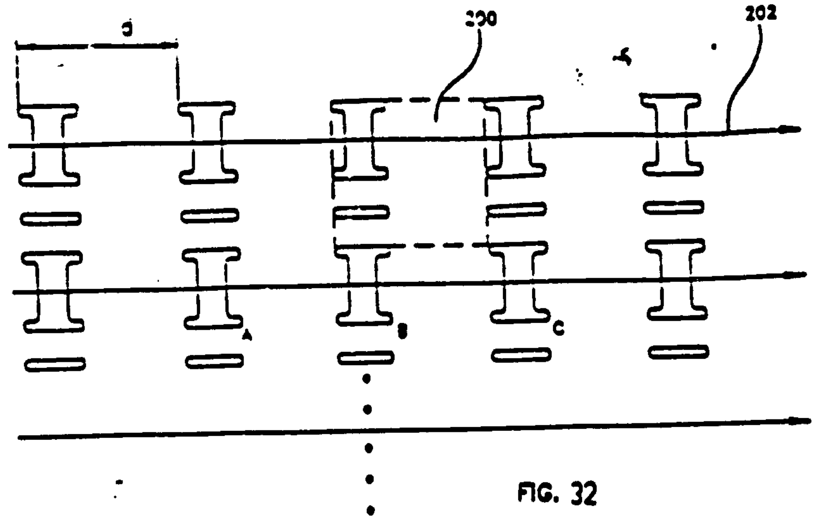

FIG. 32

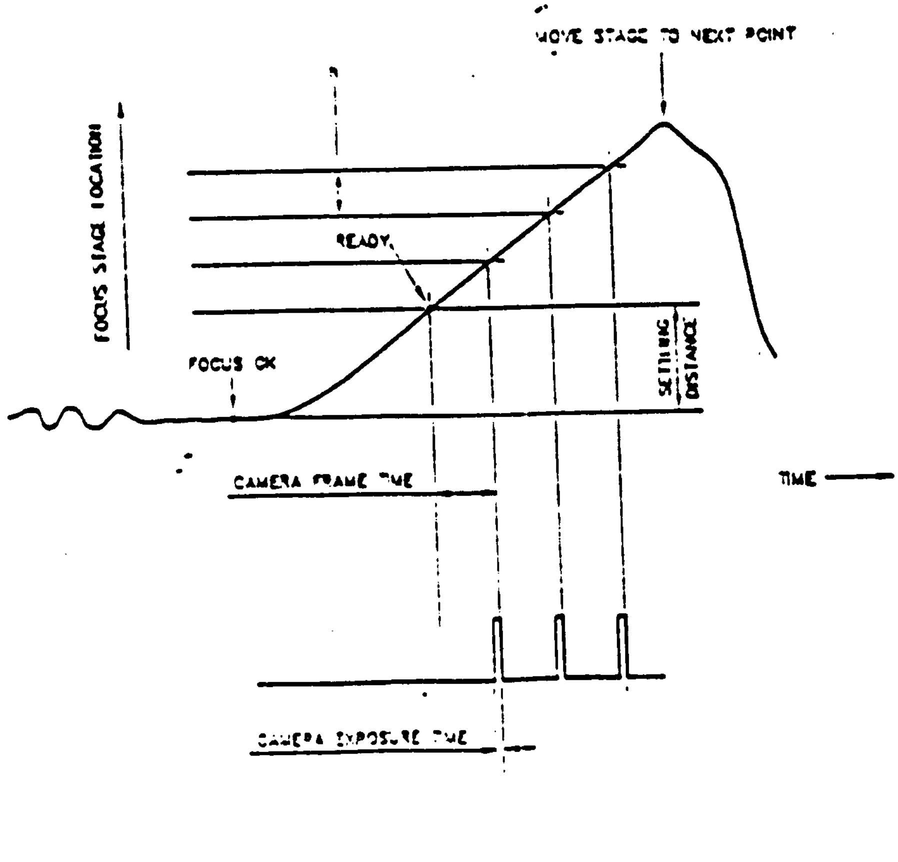

FIG. 37

Phase 1 I.P. OverAll Functional Block Diagram
(Repetitive Pattern Inspection)

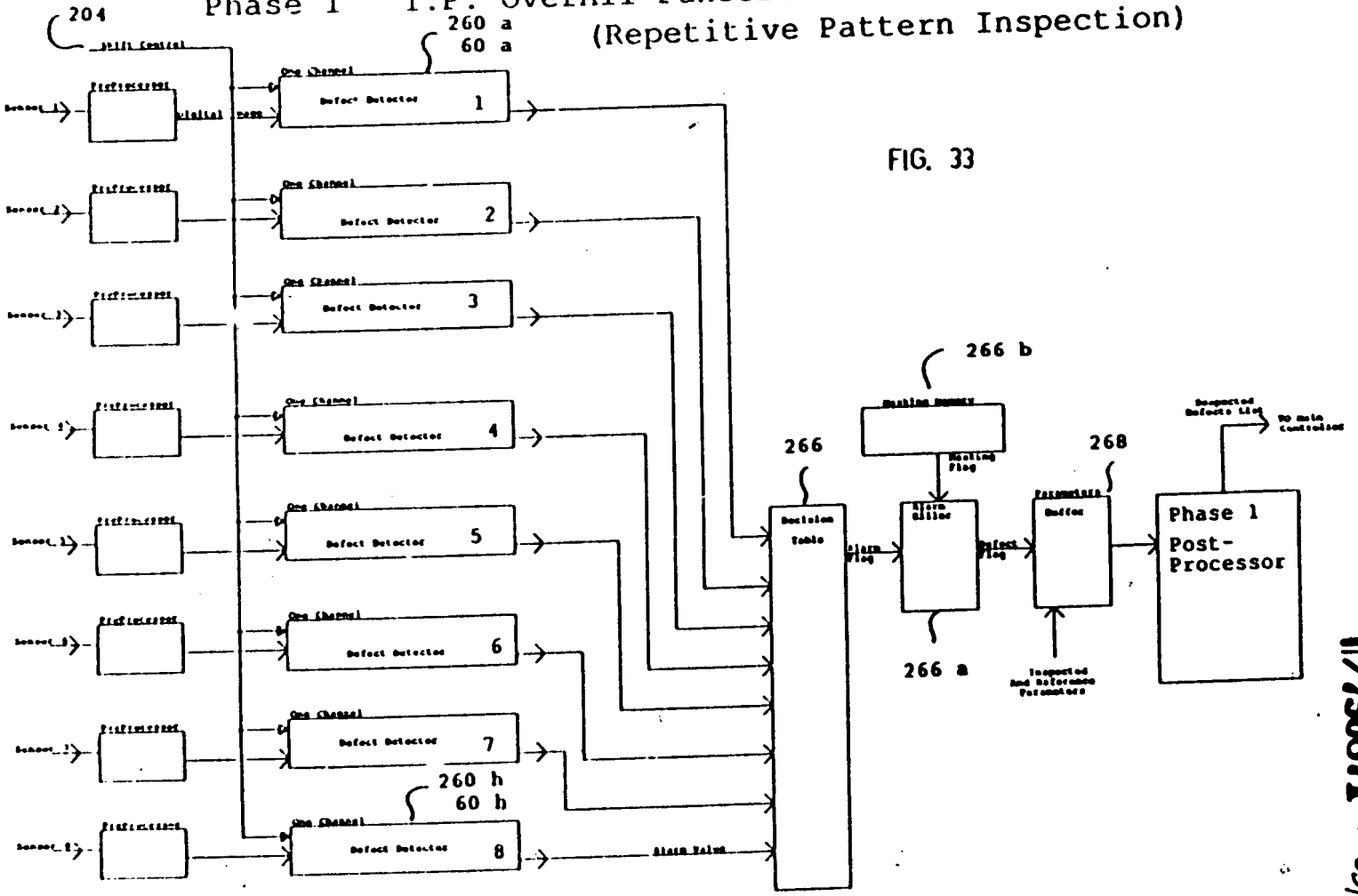

FIG. 33

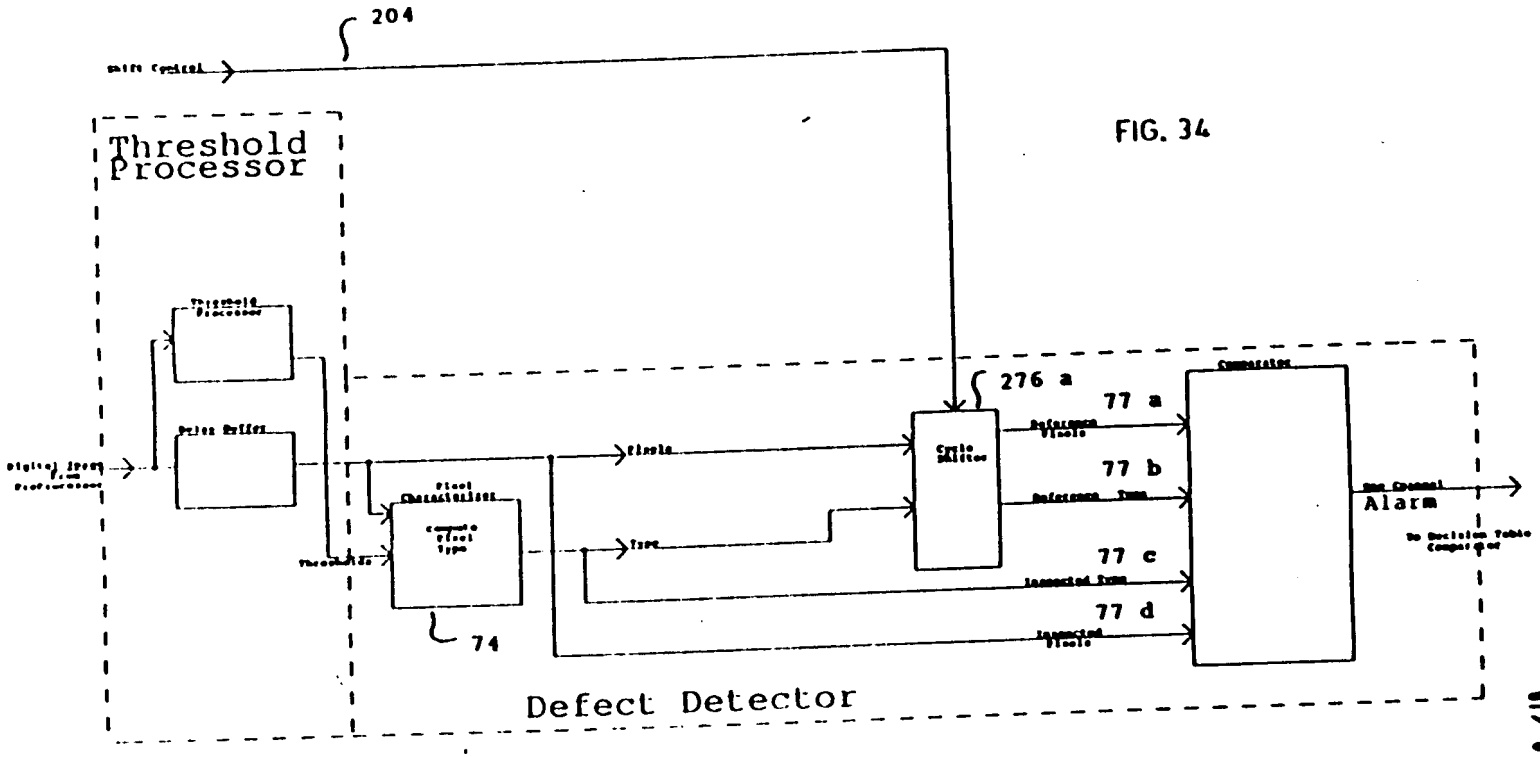

FIG. 34

One Channel I.P. Block Diagram

(Repetitive Pattern Inspection)

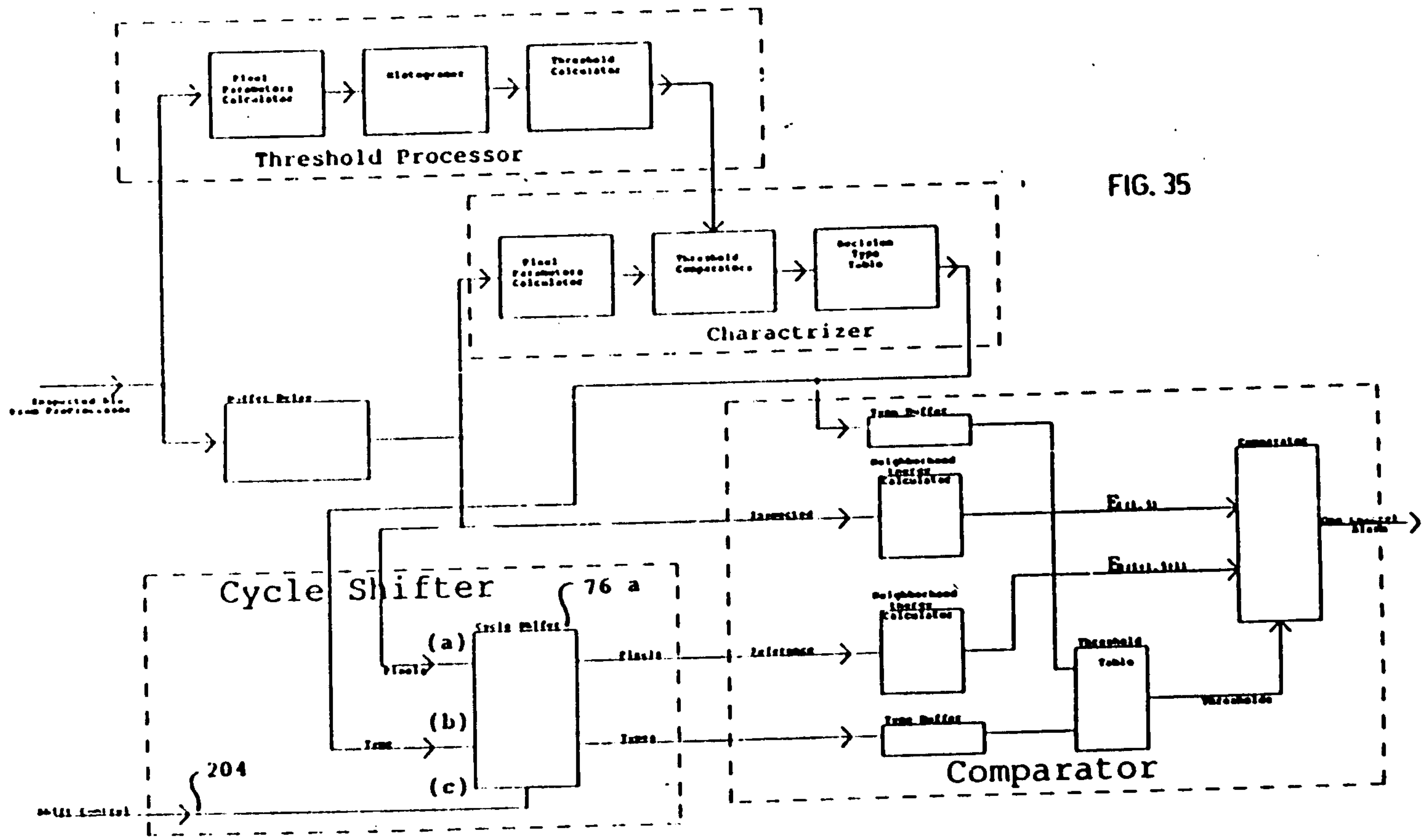

FIG. 35

Defect Detector Block Diagram
(Repetitive Pattern Inspection)

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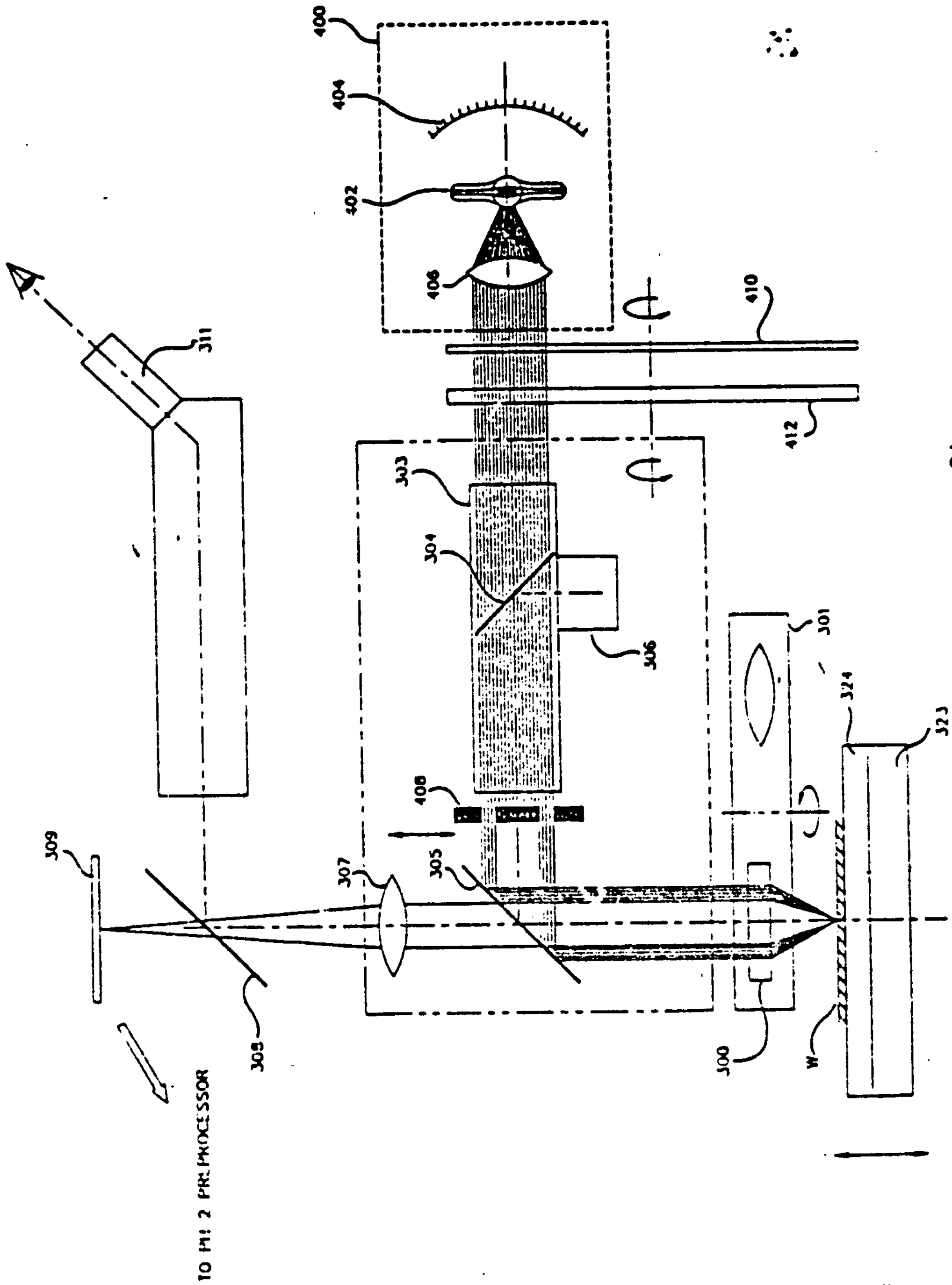

FIG. 36

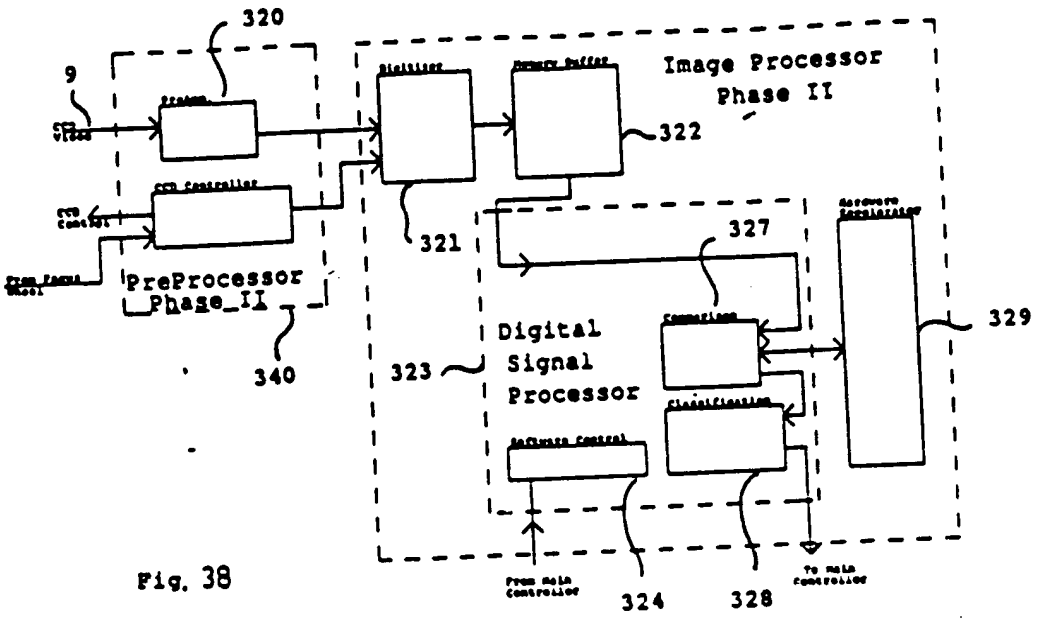
320
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Image Processor
Phase II
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327
329
PreProcessor
Phase_II
340
Digital
Signal
Processor
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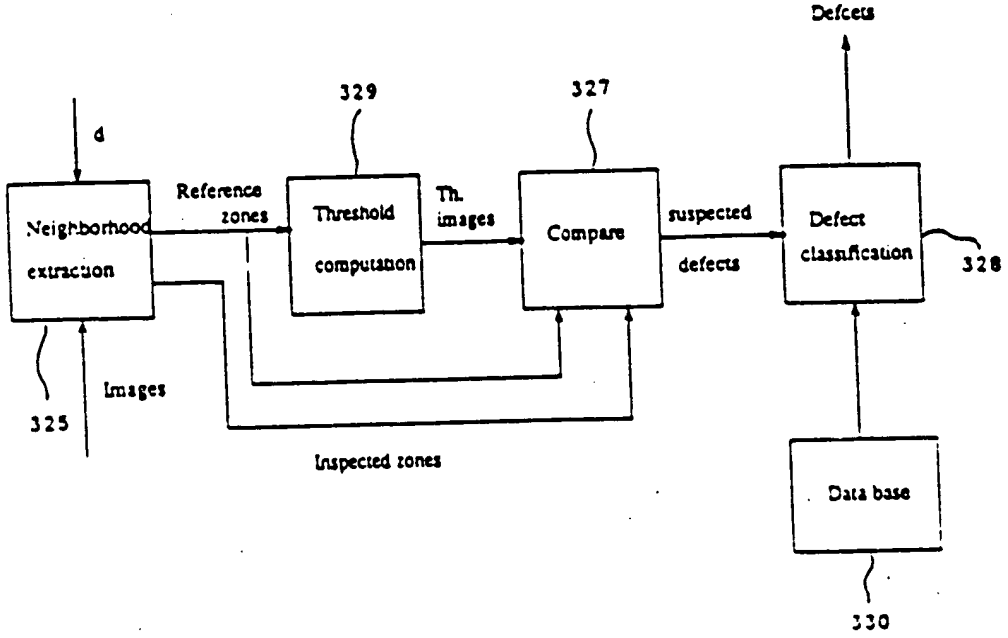
Fig. 38


Defects
329
327
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Reference
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328
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Images
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Inspected zones
Data base
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Fig. 39

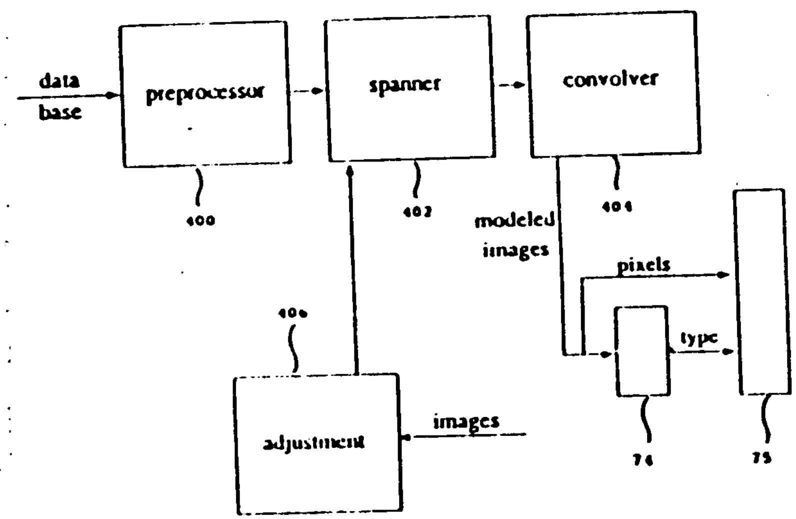


FIG. 40

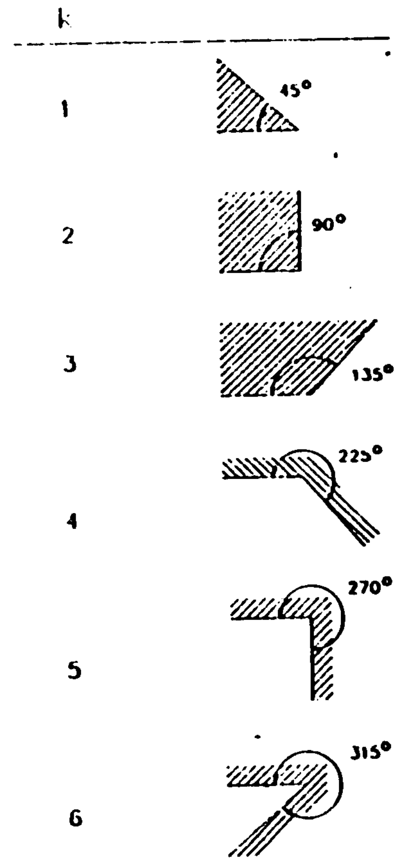


FIG. 41

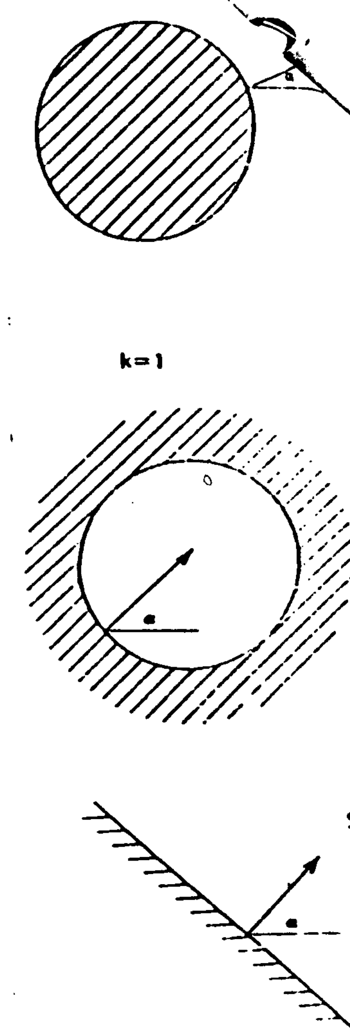
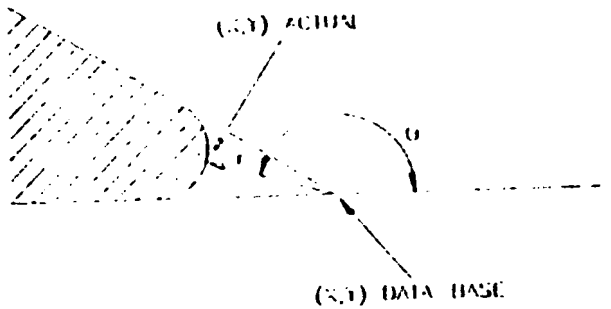


FIG. 42



CORNER SHIFT

FIG. 44

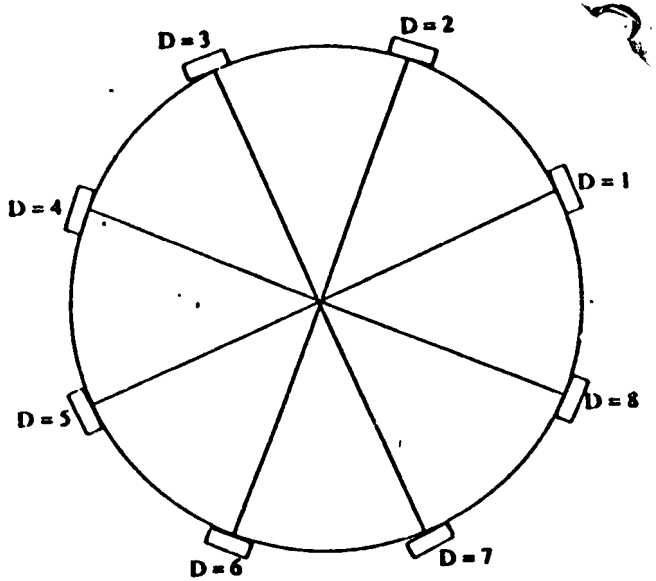


Fig. 43

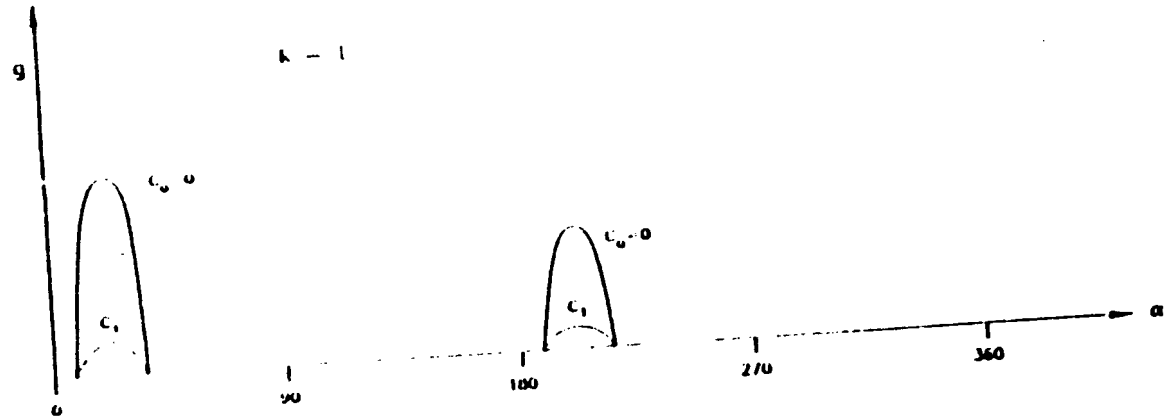


FIG. 45

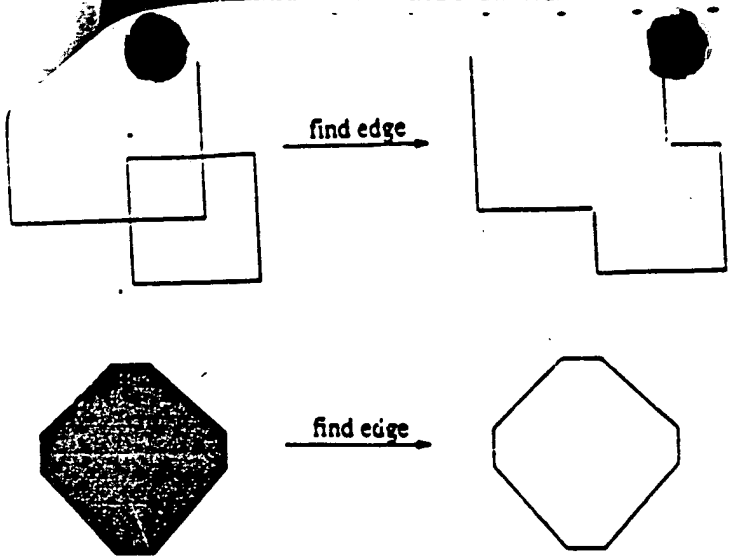


Fig. 46

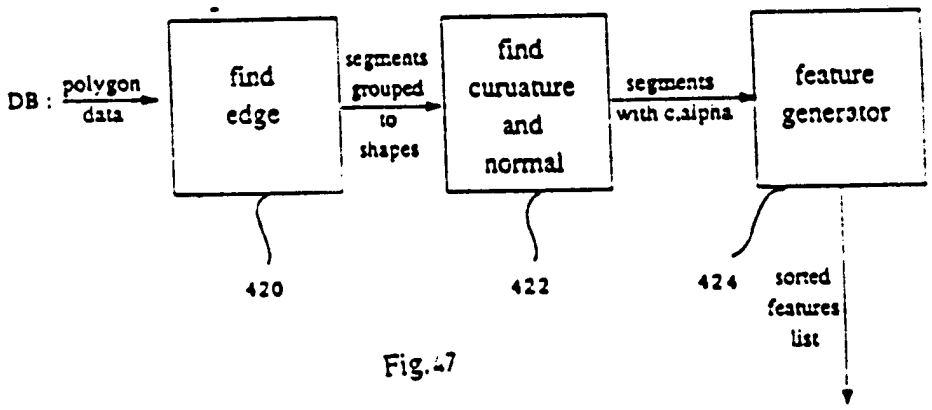


Fig. 47

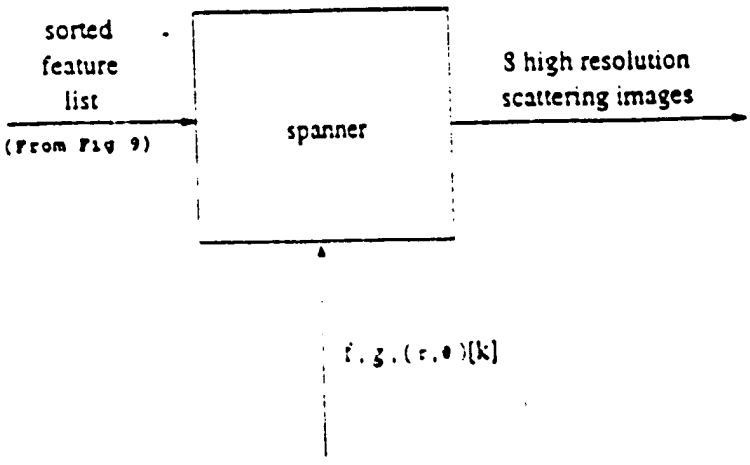


Fig. 48

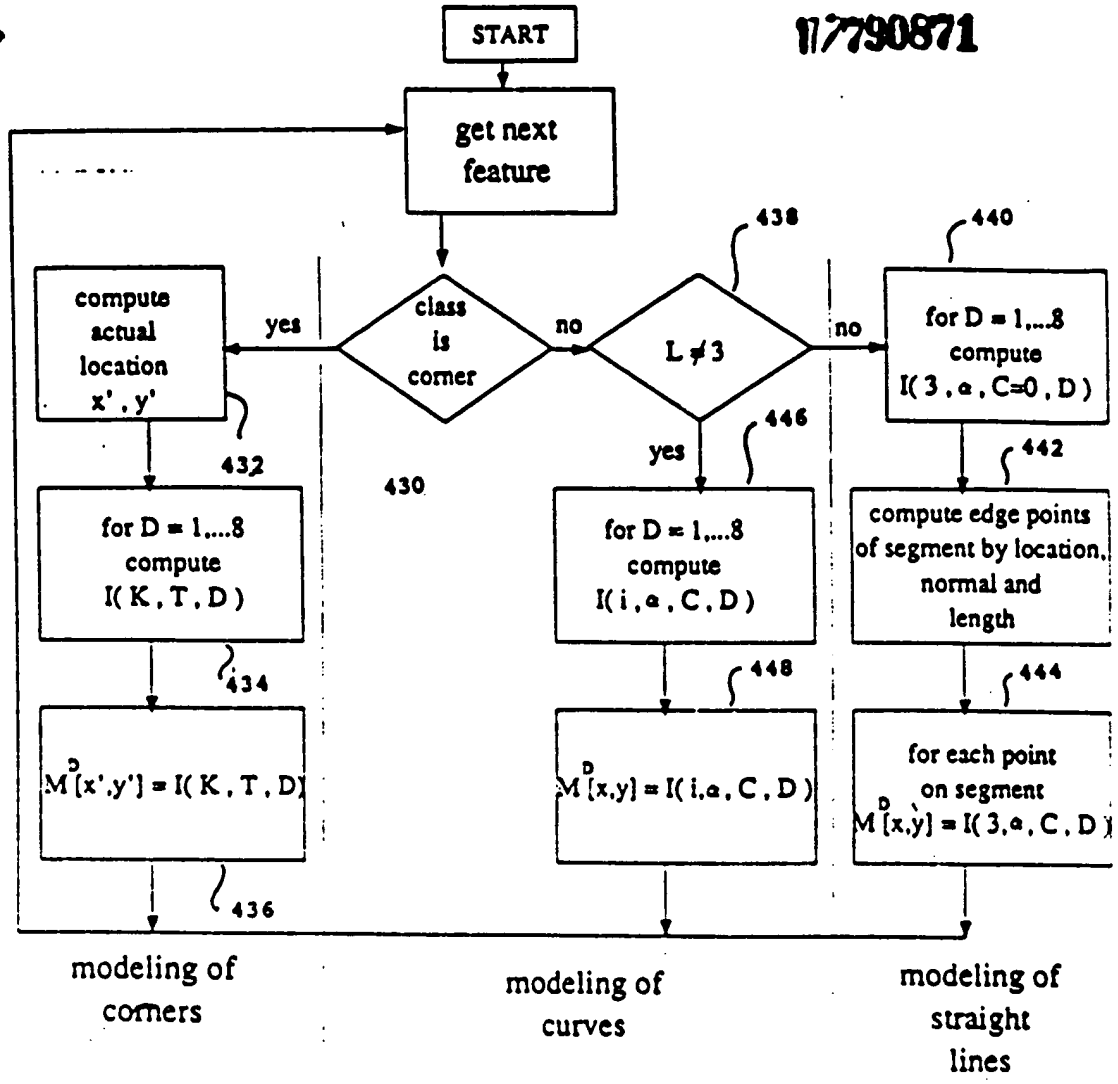


Fig. 9 : spanner flow-chart